Gate Commutated Thyristor With Voltage Independent Maximum Controllable Current

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***Abstract*— In this letter, we use a novel 3-D model, earlier calibrated with experimental results on standard gate commutated thyristors (GCTs), with the aim to explain the physics behind the high-power technology (HPT) GCT, to investigate what impact this design would have on 24 mm diameter GCTs, and to clarify the mechanisms that limit safe switching at different dc-link voltages. The 3-D simulation results show that the HPT design can increase the maximum controllable current in 24 mm diameter devices beyond the realm of GCT switching, known as the hard-drive limit. It is proposed that the maximum controllable current becomes independent of the dc-link voltage for the complete range of operating voltage.**

***Index Terms*— Gate commutated thyristor, maximum controllable current, safe operating area, thyristor, wafer modeling.**

I. Introduction

THE integrated gate commutated thyristor is the power device of choice in high-power applications such as converters for offshore wind farms and megawatt electric motor drives. The gate commutated thyristor (GCT) was introduced in 1996 as a device with the power and current capability of a thyristor, but with the switching mechanism and performance of a transistor [1]. Simulation and experimental studies have shown that in GCTs, the limit in controllable current is a result of unequal current distribution during turn-off in combination with the effects of dynamic avalanche. As a result a drop in the maximum controllable current (MCC) density is observed with a) the increase of the device area and b) the operating dc-link voltage [2]–[7]. In 2008, the high-power technology (HPT) was introduced in Ø91 mm wafer GCTs as the best solution for the sublinear scaling of the current controllability with wafer area [8]. The makeup of a single HPT GCT cell is compared with the conventional design in Fig. 1. The corrugation in the HPT deep p-base is the result of masking the cathode regions while carrying an extra p-type implantation step [8]. Here we use a novel 3-D method (built on Synopsys TCAD) for full wafer device modeling to identify what impact the HPT would have on Ø24 mm GCTs while at the same time providing a better understanding the physics of HPT devices. This model was originally developed and calibrated by us for conventional GCTs. Hence, our findings are directly comparable with the set of experimental and simulation data of the standard GCT devices [4].

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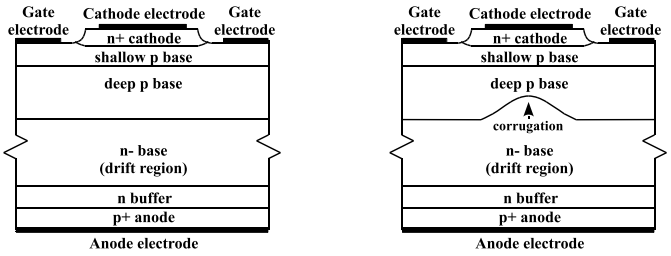


Fig. 1. Conventional and HPT cell design. (a) Conventional. (b) HPT.

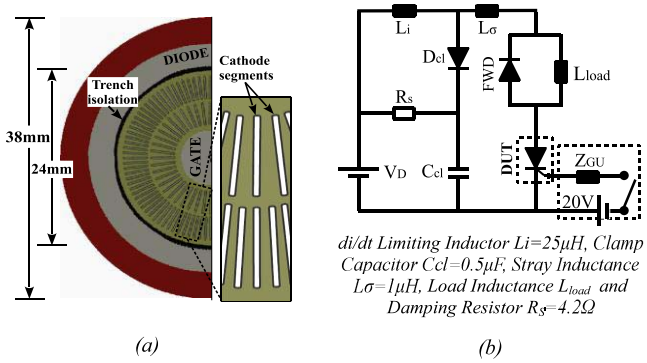


Fig. 2. Device under test with the external circuit. (a) 38mm Reverse-Conducting IGCT semiconductor. (b) External circuit used for MCC measurements.

II. Simulation Experiment Setup

The reference device used for this letter [Fig. 2(a)] is a conventional ABB 4.5 kV reverse-conducting GCT with a diameter of 38 mm. The GCT part of the device has an active area of 3.5 cm^2 and a diameter of 24 mm.

The 3-D model of the HPT wafer device (Fig. 3) features a gate electrode split in two concentric regions, each one surrounding the cathode fingers of the equivalent concentric ring, in order to facilitate variable gate impedance. Z_{G1} and Z_{G2} account for the uneven gate impedance load due to the gate metallization [8]. The anode electrode is also split in two concentric regions. The split anode arrangement enables a quick way to evaluate the current distribution inside the wafer during turn-off. The cathode fingers are shorted together to form the cathode contact of the GCT.

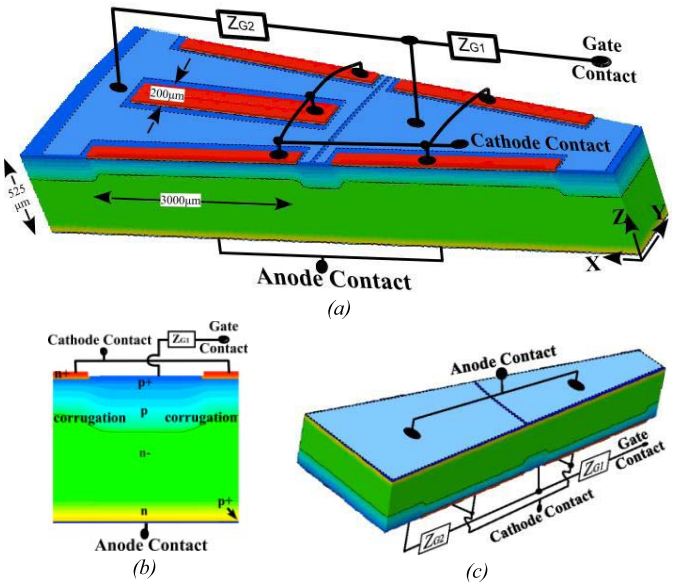


Fig. 3. Angular slice of the 3-D simulation domain with the parasitic gate impedances composed of a series connection of gate resistances (R_{G1} = 0.65 mΩ, R_{G2} = 0.85 mΩ) and inductances (L_{G1} = 0.4 nH, L_{G2} = 0.6 nH). (a) Cathode side up. (b) Device structure along a plane cut across the X-axis. (c) Anode side up.

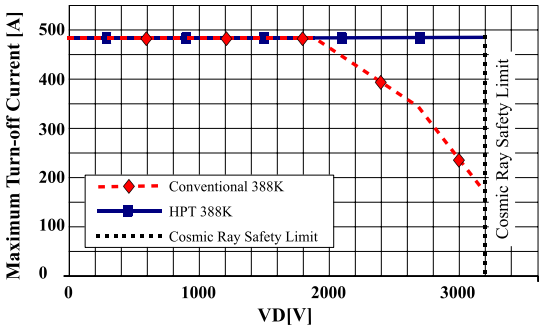
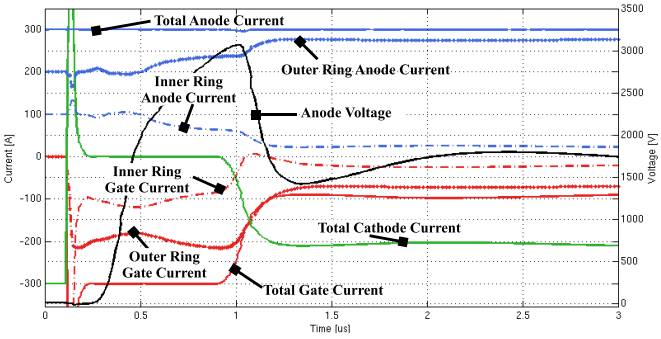
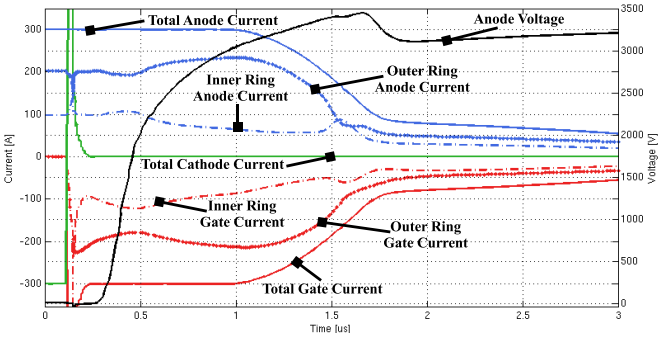


Fig. 4. Turn off current capability at dc-link voltage (VD) for the conventional and the HPT design.



(a) Conventional MCC failure to turn-off waveform



(b) HPT successful turn-off

Fig. 5. Turn-off waveforms for (a) conventional and (b) HPT at VD = 3000V, Ion = 300A, TJ = 388 K.

The determination of the maximum turn-off current requires a large number of mixed mode simulations because one simulation can only predict whether the device is able to switch off or not. For every dc link voltage (VD) the junction temperature is fixed, the circuit components are kept constant and the device is turned off at different certain current levels. Every successful turn-off simulation is followed by another turn-off where the current is increased until an MCC failure is recorded. In simulations a turn-off is considered to be successful when (i) at the end of the turn-off tail the anode current reduces to the typically low leakage off-state current (ii) and at any time during the turn-off process the current through any of the cathode fingers does not conduct more than 10% of its on-state current level. The second condition is imposed to fulfill the hard-drive condition. The test circuit is shown in Fig. 2(b).

III. Results and Analysis

The MCC simulation results for the HPT device at 388K are compared in Fig. 4 with those of a standard GCT. For the conventional GCT they are in good agreement with experimental results [4], [5]. For low dc-link voltages (VD < 1900 V), the failure mechanism is triggered by the violation of the hard drive requirement whereas at higher voltage range (VD > 1900 V), the mechanism that dominates is avalanche driven. As shown in Fig. 4, the MCC of the conventional GCT is reduced from the hard-line (i.e. the maximum of MCC in Fig. 4) by 30% at normal operating dc-link voltages (e.g. 2.7 kV) and by about 60% at high dc-link voltages (e.g. 3 kV). The HPT has the same current controllability with the conventional GCT at low-voltage operation (VD < 1900 V), enforced by the hard drive limit. However it is not subject to a destructive mechanism due to dynamic avalanche at higher voltage operation (VD > 1900 V), not even at the highest simulated VD = 3200 V; condition at which the carriers ionization is very strong. Instead, the final destruction mechanism is still caused by the violation of hard drive operation, similar to the low-voltage operation.

The turn-off characteristic waveforms of the conventional GCT and the HPT at TJ = 388 K, VD = 3000 V and Ion = 300 A are depicted in Fig. 5 and the carriers' density maps during turn-off in Fig. 6. When the blocking voltage reaches values above 1.9 kV, the GCT enters an avalanche-transistor positive feedback current gain mechanism where the current generated by the dynamic avalanche serves as the base of the p-n-p part of the device, resulting in a lower differential resistance [4], [5].

The current redistribution within the wafer of the device (anode current waveforms of Fig. 5) indicates that this mechanism is stronger in the segments farther from the gate contact. It can only partly be mitigated by means of lateral lifetime control [9] and the design of emitters of variable width [3]. The increase in the current density locally, triggers the n+ cathode in the conventional GCT design. The combined

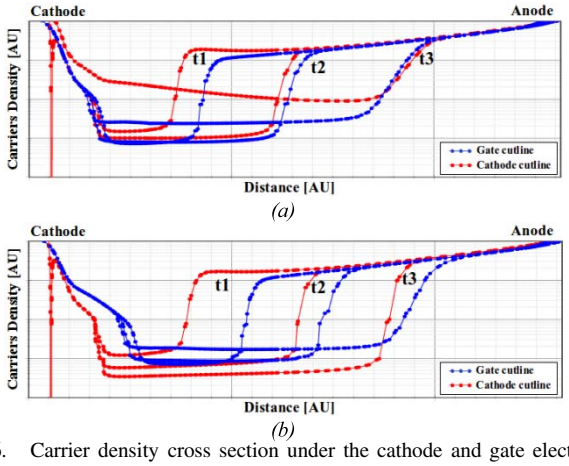


Fig. 6. Carrier density cross section under the cathode and gate electrodes at t1 = 0.4μs, t2 = 0.7μs and t3 = 1μs. (a) Conventional design. (b) HPT design.

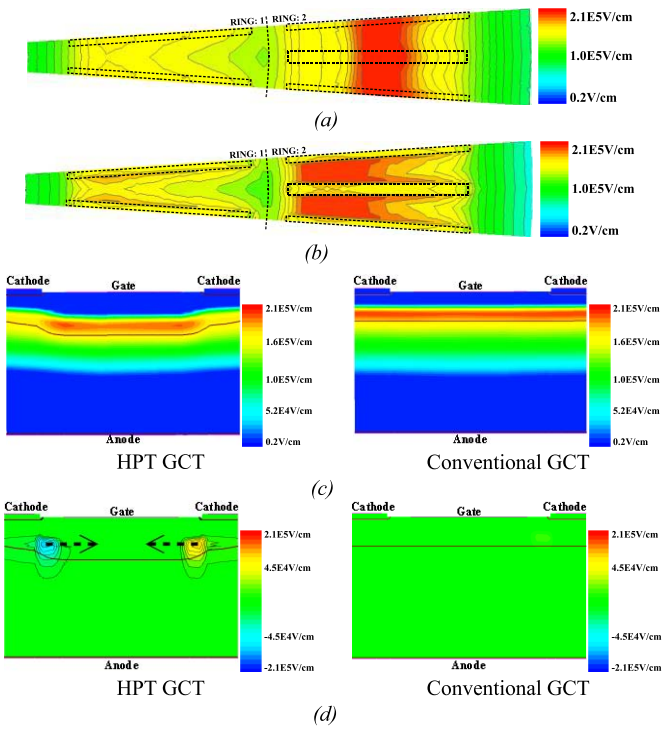


Fig. 7. Electric field contours during turn-off in the HPT and the Conventional GCT. (a) Conventional GCT: Absolute Electric Field (p-base/n-base junction, z-axis cutplane). (b) HPT GCT: Absolute Electric Field (p-base/n-base junction, z-axis cutplane). (c) Vertical Component of Electric Field (Ring 2, x-axis cutplane). (d) Lateral Component of Electric Field (Ring 2, x-axis cutplane).

avalanche-transistor / transistor-transistor positive current gain mechanism [5] enforces the final destruction. The HPT design however, does not show indications of cathode retriggering. Even though both the current redistribution and the dynamic avalanche carrier generation are indeed very strong, the HPT GCT turns off safely.

Fig. 7 illustrates the electric field contours for the two GCT variants when the dynamic avalanche phenomenon is at its maximum. It depicts z-cut and x-cut planes of the numerical devices at the time instance in Fig. 5 where the devices support 2.7 kV. As shown, the electric field is higher in the remotest segment regions (ring 2), both for the conventional and the HPT GCT because of a higher current density at the outermost ring. This induces an imbalanced dynamic avalanche carrier generation which alters even more the conduction current share between the innermost and outermost rings (also depicted in the waveforms of Anode current in Fig. 5). In the HPT however, the peak vertical component of the electric field and hence the location of strong dynamic avalanche carriers generation is "contained" in regions located underneath the gate (rather than the cathode) electrode [Fig. 7(b) and 7(c)].

Furthermore, the structured junction in HPT creates a lateral component of the electric field which points toward the gate electrode. This does not appear in the conventional design [Fig. (7d)]. The lateral electric field component in the HPT GCT design redirects the hole current toward the gate contact, resulting in a more preferable current path as the holes are prevented from reaching the proximity of the cathode junction.The combination of the aforementioned phenomena results in preventing the dynamic avalanche current to ignite the combined avalanche-transistor/transistor-transistor current gain mechanism. Therefore, the HPT design manages to suppress the adverse effects of the voltage dependent dynamic avalanche to such an extent that the MCC becomes independent of the dc link voltage, allowing for an invariable MCC for the complete locus of operating voltage.

IV. Conclusion

An accurate 3-D wafer level simulation tool was used in this letter to analyze how the HPT design would affect the performance of Ø24 mm GCTs. Furthermore, we give a complete explanation of the physics that govern the operation of HPT GCTs. In particular we show that a 24 mm in diameter corrugated p-base GCT can achieve a voltage-independent MCC because of its immunity to dynamic avalancheat high dc-link voltages. The MCC in such a case is only limited by the requirements for the hard drive which is independent of the VD. As a result, when compared to a conventional GCT, the safe operating current level in an HPT GCT can be increased by more than 240% at the highest operational dc voltages.

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