On the 3C-SiC/SiO_2 n-MOS interface and the creation of a calibrated model for the Electrons' Inversion Layer Mobility covering a wide range of operating temperatures and applied gate voltage

Neophytos Lophitis
Faculty of Engineering
University of Nottingham
Nottingham, UK
neo.lophitis@nottingham.ac.uk

Anastasios Arvanitopoulos
Power and Sensor Systems
Infineon Technologies Austria AG
Villach, Austria
a.e.arvanitopoulos@ieee.org

Mike R. Jennings
College of Engineering
Swansea University
Swansea, UK
m.r.jennings@swansea.ac.uk

Philip A. Mawby
School of Engineering
University of Warwick
Coventry, UK
p.a.mawby@warwick.ac.uk

Marina Antoniou
School of Engineering
University of Warwick
Coventry, UK
marina.antoniou@warwick.ac.uk

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***Abstract*—Cubic (3C-) silicon carbide (SiC) metal oxide semiconductor (MOS) devices have the potential to achieve superior performance and reliability. The effective channel mobility can be significantly higher compared to other SiC polytypes due to the smaller concentration of active SiC/SiO_2 interface traps and the gate leakage current can be smaller than other SiC polytypes and silicon (Si) because of the more favourable conduction band offset between 3C-SiC and silicon dioxide (SiO_2). This work examines the 3C-SiC/SiO_2 n-MOS interface and makes use of three independent sets of experimental data to derive and validate a comprehensive model of the inversion layer mobility in 3C-SiC n-MOS structures. The model derived in this work can be used by technology computer aided design (TCAD) tools and can predict the channel mobility with reasonable accuracy for gate voltages ranging 0V - 20V, and for temperatures ranging 300K - 473K. The ability to reproduce correctly the physical phenomena affecting the 3C-SiC/SiO_2 n-MOS channel mobility in TCAD through an appropriately parameterised model is imperative for the design and optimization of MOS devices like MOSFETs and IGBTs and the further development of 3C-SiC device technology.**

Keywords— Cubic, Silicon Carbide, 3C-, SiC, channel mobility, Metal Oxide Semiconductor, MOS, TCAD, model

I. Introduction

When compared to the more mature hexagonal SiC polytypes (4H-, 6H-), 3C-SiC is a Wide Band Gap (WBG) semiconductor with desirable advantages. The ability to grow 3C-SiC on large area Si wafers makes it a low cost alternative, whereas its isotropic properties [1] combined with a reduced population of active $3C - SiC/SiO_2$ interface traps (D_{it}^{3C-SiC/SiO_2}), allows for high effective channel mobility in MOS devices, with reported values of up to 260 cm^2/Vs [2]–[5]. Importantly, the conduction band offset of 3C-SiC with SiO_2 is 3.7 eV, which is larger compared to the band offset of Si, 6H- and 4H- SiC with SiO_2 (3.2, 2.95, 2.7 eV respectively [6]). The larger conduction band offset can result in a reduced gate leakage current at any given oxide electric field due to reduced Fowler-Nordheim (F-N) tunnelling mechanism. Consequently, 3C-SiC MOS devices show a real competitive advantage potential.

Recently, 3C-SiC on silicon (Si) substrates with defects density below $400cm^{-1}$ and a 600V vertical Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with specific on-resistance of 8.2 $m\Omega cm^2$ were demonstrated [7], [8]. Further, a comprehensive set of physics models for TCAD tools of bulk 3C-SiC [9]–[12] was developed, enabling the numerical and physical study, as well as the optimization of 3C-SiC devices [13]–[18]. In this work we report on the physics and TCAD model of the inversion layer electrons' mobility, with scope to allow for more representative simulations of devices with 3C-SiC/SiO_2 regions [15], [17]. It accounts for the complex contribution of multiple mobility reduction factors. Measurements from 3C-SiC MOSFETs [19]–[21] are utilized for the development and evaluation of the model.

II. Physics of the $3C - SiC/SiO_2$ Interface

The quality of SiO_2 grown on SiC is comparable to SiO_2 grown on Si [22], [23] but due to the presence of the carbon atoms in SiC, the density of states (D_{it}) at the SiC/SiO_2 interface is higher [24]–[27]. According to the carbon cluster model [28], the SiC/SiO_2 interface is a defect rich region populated by π-bonds, sp^2-bonded carbon clusters, Near Interface Traps (NITs) and fixed charges (Q_f). Significantly, NITs are acceptor-like defects characterized by fast trapping abilities [29] obstructing the transport of electrons in the channel, eventually resulting in poor performance, whilst raising oxide reliability concerns [30]

In 4H-SiC MOSFETs, NITs are located within the band gap close to E_C and largely affect the channel mobility [29], [31], [32]. Recent research suggests that more elaborate gate oxide fabrication processes (e.g. forming a SiO_2/Al_2O_3 gate stack) are required to reduce the defects at the 4H-SiC/SiO_2 interface, the defects [33]. This is not needed for the 3C-SiC/SiO_2 interface. As shown in Fig. 1, for a 3C-SiC/SiO2 n-MOS structure the NITs and all the acceptor-like traps are above the conduction band (E_C) of 3C-SiC [34]–[36]. Consequently, only Q_f and donor-like traps (π-bonds and sp^2

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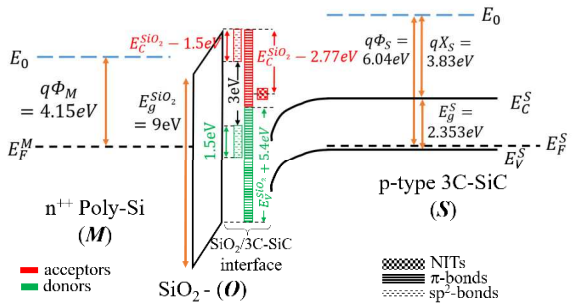

Fig. 1 Energy band diagram for n-type 3C-SiC MOS at V_G = 0V showing the D_{it}^{3C-SiC/SiO_2} according to the carbon cluster model [28] for 3C-SiC/SiO_2. The figure does not illustrate the acting Q_f^{3C-SiC}.

-bonds) can affect the electrical properties [37], [38]. In addition to existing Q_f, ionized donor-like states are highly likely to be occupied by a hole and hence also act as fixed positive charges at the interface. Nonetheless, the position of the Fermi-level (E_F) at the interface during thermal equilibrium defines only a limited part of donor-like D_{it}^{3C-SiC/SiO_2} to be energetically above it (i.e. they are ionized). In addition, with application of positive bias on the gate, the amount of ionized D_{it}^{3C-SiC/SiO_2} reduces because the bands at the interface bend further downwards. Therefore, the importance of D_{it}^{3C-SiC/SiO_2} on affecting the mobility of electrons in the channel of 3C-SiC n-MOS devices can be considered negligible compared to the effect from Q_f [29], [39], [40].

III. 3C − SiC/SiO_2 Channel Mobility Model

The mobility of electrons in the channel can be modelled by deploying Matthiessen's rule as a weighted summation of different mobility components (1). These include the bulk mobility (μ_{bulk}^{3C-SiC}), acoustic phonon scattering (μ_{ac}^{3C-SiC}), surface roughness scattering (μ_{SR}^{3C-SiC}) and coulomb scattering on Q_f and ionized traps at the interface (μ_{cb}^{3C-SiC}). In (1), D is a damping parameter defined as $D = e^{-x/l_{crit}}$, where x is the distance from the interface and l_{crit} is a fitting parameter. D ensures that the inversion layer terms on calculating the corresponding mobility degradation elements are switched off far from the channel region area.

$$\frac{1}{\mu_{ch}} = \frac{1}{\mu_{bulk}} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{SR}} + \frac{1}{\mu_{cb}} \quad (1)$$

The parameters and models used for μ_{bulk}^{3C-SiC}, which comprises the mobility dependence on doping (μ_{dop}^{3C-SiC}) and electric field parallel to the current flow ($\mu_{E//}^{3C-SiC}$), are those in [12]. The focus of this work is on the remaining contributions in (1) which describe the mobility reduction at the semiconductor/oxide interface, where the transverse electric field ($E_\perp$) is the driving force. The Lombardi equations (2), (3) and (4) [41] are utilized to model the μ_{ac}^{3C-SiC} and μ_{SR}^{3C-SiC}, whilst (5) models the μ_{cb}^{3C-SiC}.

$$\mu_{ac} = \frac{B}{E_\perp} + \frac{CN_A^\lambda}{E_\perp^{1/3}\left(\frac{T}{300}\right)^{k1}} \quad (2)$$

$$\mu_{SR} = \left(\frac{E_\perp^{A^*}}{\delta} + \frac{E_\perp^3}{\eta}\right)^{-1} \quad (3)$$

$$A^* = A_{init} + \frac{(\alpha_{\perp,n} n + \alpha_{\perp,p} p) N_{ref}^\beta}{N_A^\beta} \quad (4)$$

$$\mu_{cb} = \frac{\mu_1 \left(\frac{T}{300}\right)^{k2} \left\{1 + \left[n \Big/ \left(n_{trans}\left(\frac{Q_f}{N_0}\right)^{\eta_1}\right)\right]^v\right\}}{\left(\frac{Q_f}{N_0}\right)^{\eta_2} e^{-(d_{init}/l_{crit})} \left(1 - e^{-\left(E_\perp/E_0\right)^\gamma}\right)} \quad (5)$$

IV. Model Parameters at 300K

The parameters affecting the electrical performance of a MOS- structure include the p-body doping (N_A), the oxide thickness (T_{ox}), the gate metal workfunction (Φ_M) and the Q_f. The analysis and incorporation of the carbon cluster model for the case of 3C-SiC/SiO_2, conducted in Section II, suggest that the impact of D_{it} is minor, and has thus been omitted. On calibrating the mobility model (1) for 3C-SiC n-MOS interfaces at 300K, two sets of measurements are employed from n-MOS devices having different designs.

Device **n-MOS A** is a 3C-SiC n-MOS structure featuring poly-Si as gate metal, $T_{ox}^A = 60nm$ SiO_2 gate oxide and $Q_{f,A}^{3C-SiC} = 3.9 \times 10^{11} cm^{-2}$, whilst N_A^A is not provided [19]. Device **n-MOS B** comprises a 3C-SiC grown on Si (3C-SiC-on-Si) n-MOS with poly-Si as gate metal, $N_A^B = 2 \times 10^{17} cm^{-3}$ and $T_{ox}^B = 80nm$ SiO2 gate oxide, whilst the $Q_{f,B}^{3C-SiC}$ is not provided [20]. The measured channel mobility (μ_{ch}) as a function of the applied gate voltage (V_G) for the two MOS structures is given in Fig. 2 and Fig. 3. The gate threshold voltage (V_{th}) for this work is determined to be the V_G at the onset of inversion, (i.e. where the mobility value becomes non-zero) in the $\mu_{ch} - V_G$ plots. For n-MOS A $V_{th}^A \approx 5V$ and for n-MOS B $V_{th}^A \approx -0.5V$. The N_A^A and $Q_{f,B}$ values are then calculated, using (6)-(9) and the material parameter information of Table I to be $N_A^A = 2.5 \times 10^{17} \mathrm{cm}^{-3}$ and $Q_{f,B} = 2.3 \times 10^{12} cm^{-2}$.

$$V_{th} = V_{FB} + \frac{T_{ox}|Q_{inv}|}{\epsilon_{ox}} + \Phi_t \quad (6)$$

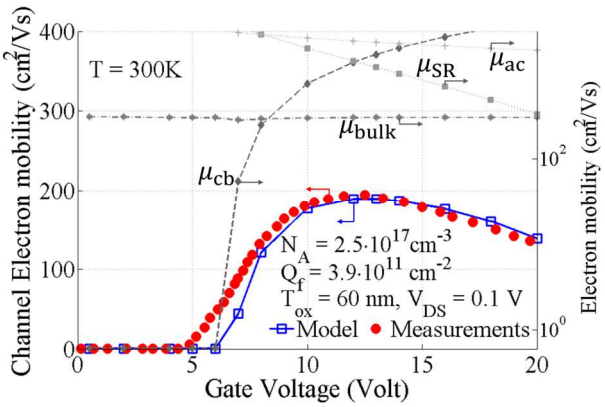

Fig. 2 Channel mobility as a function of gate voltage at 300K for n-MOS A. Simulations results of the channel mobility (□) and the components of mobility (grey) using the derived model are compared to measurements (•) obtained from [19].

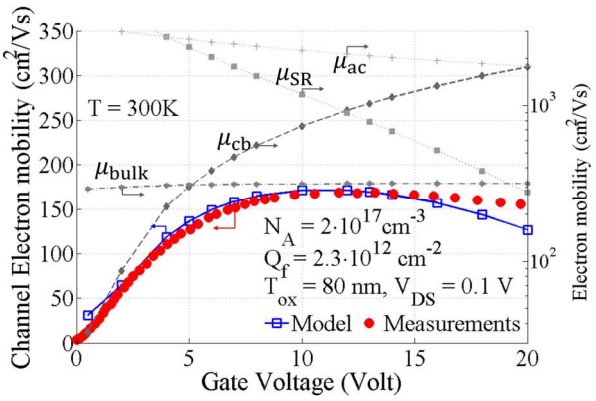

Fig. 3 Channel mobility as a function of gate voltage at 300K for n-MOS B. Simulations results of the channel mobility (□) and the components of mobility (grey) using the derived model are compared to measurements (•) obtained from [20]

$$\Phi_t = 2\frac{kT}{q}\ln\frac{N_A}{n_i} \tag{7}$$

$$V_{FB} = \Phi_M - \left(\chi_S + \frac{E_g^S}{2} + \frac{\Phi_t}{2}\right) - \frac{T_{ox}qQ_f}{\epsilon_{ox}} \tag{8}$$

$$|Q_{inv}| = \sqrt{2q\epsilon_S N_A \Phi_t} \tag{9}$$

TABLE I.
PARAMETERS USED IN THE CALCULATION OF THRESHOLD VOLTAGE

Parameter	Material	Value
$\Phi_M\ (eV)$	N – Polysilicon	4.15 [a]
$\chi_S\ (eV)$	3C-SiC	3.83 [b]
$E_g^S\ (eV)$	3C-SiC	2.35 [b]
$n_i\ (cm^{-3})$	3C-SiC	2.285×10^{-1} [b]
$\epsilon_S\ (Fcm^{-1})$	3C-SiC	0.8606×10^{-12} [b]
$\epsilon_{ox}\ (Fcm^{-1})$	SiO_2	0.3453×10^{-12} [c]

[a] [42] [b] [11] [c] [43]

To derive the parameter values presented in Table II for (2), (3), (4) and (5), precise geometric and electro-physical models of devices MOS A and B were developed using Synopsys TCAD. The properties of bulk 3C − SiC were modelled using the material physics equations and parameters discussed in [11]. The equations (2), (3), (4) and (5) were incorporated and the equivalent parameter values used for Silicon MOS devices were used as the initial model condition. Following, V_G was ramped from 0 to 20V and concurrently, the mobility driving forces ($E_\perp$, $E_{//}$), the density of free electrons (n) and the density of free holes (p) at the channel region were monitored and recorded. μ_{ch} and the individual mobility components were then calculated as a function of V_G and the simulation results were overlayed and compared with the equivalent measurements. The procedure was repeated with the parameters altered one by one to study how they influence $\mu_{ch}(V_G)$ and the individual mobility components, which allowed for the informed adjustment of the parameter values during each subsequent iteration. After multiple iterations an acceptable fit between model predictions and measurements was achieved for both devices (depicted in Fig. 2 and Fig. 3).

The simulations show that at low voltages the coulomb scattering mobility (μ_{cb}) component dominates, whereas at higher voltages the combined effect of surface scattering (μ_{SR}) and bulk mobility (μ_{bulk}) dominates. As the gate voltage increases further, surface scattering dominates. As depicted, the model slightly overestimates the μ_{cb} component for the n-MOS A case whereas it slightly overestimates the μSR term for the case of n-MOS B. When considering the rather wide range of applied gate voltages examined and the large dissimilarity of the two structures used for the model parameters derivation, the overall model prediction can be considered sufficiently credible for general use with 3C-SiC n-MOS devices.

V. TEMPERATURE DEPENDENCE

The temperature dependence of the proposed mobility model makes use of measurements from a third MOS structure, MOS C [21]. MOS C has identical epilayers with those of MOS A (i.e. $N_A^C = N_A^A$). Its oxide thickness is $T_{ox} = 64nm$ whereas from the measurements shown in Fig. 4 it can be estimated that $V_{th}^C \approx 1.5V$. From (6)-(9) the fixed charge at the interface is calculated $Q_{f,C}^{3C-SiC} = 1.8 \times 10^{12} cm^{-2}$. By following the same procedure described in Section IV, the model parameters k_1 and k_2 listed in Table II have been derived. As shown, in Fig. 4 the predictions are in sufficient agreement with the measurements for the temperature range 300K - 473K, with the model moderately overestimating the mobility at 300K and moderately underestimating it at 473K.

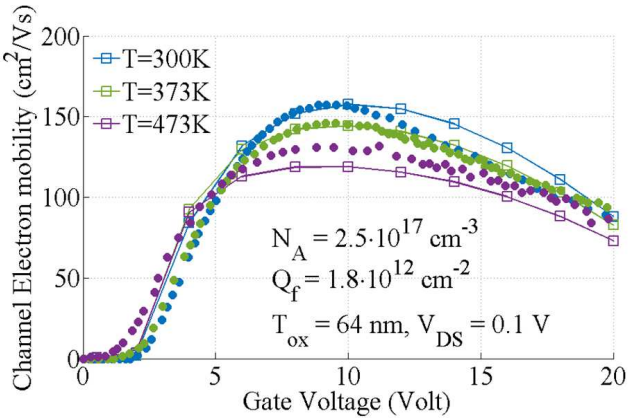

Fig. 4 Channel mobility as a function of gate voltage between 300K and 473K for n-MOS C. Simulations results using the derived model (□) are compared to measurements (•) obtained from [21]

TABLE II.
PARAMETER VALUES OF THE CHANNEL MOBILITY MODEL

Parameter	Eq.	Value
$B\ (cm\,s^{-1})$	(2)	5×10^8
C $(cm^{\frac{5}{3}}\,V^{-\frac{2}{3}}\,s^{-1})$	(2)	5×10^2
λ	(2)	0.1
δ $(cm^2V^{-1}s^{-1})$	(3)	5×10^{16}
η $(V^2cm^{-1}s^{-1})$	(3)	3×10^{20}

A_{init}	(4)	2.1
$\alpha_{\perp,n}$ (cm^3)	(4)	6.85×10^{-21}
$\alpha_{\perp,p}$ (cm^3)	(4)	6.85×10^{-21}
N_{ref} (cm^{-3})	(4)	1
β	(4)	0.092
k_1	(2)	5
E_0 (Vcm^{-1})	(5)	1×10^{-6}
N_0 (cm^{-2})	(5)	1×10^{11}
γ	(5)	1
μ_1 $(cm^2V^{-1}s^{-1})$	(5)	1
n_{trans} (cm^{-3})	(5)	2×10^{16}
η_1	(5)	0.1
η_2	(5)	0.4
v	(5)	1.2
d_{init} (cm)	(5)	5×10^{-8}
l_{crit} (cm)	(5)	7×10^{-7}
k_2	(5)	1.5

VI. Conclusions

In this work, a comprehensive model of the mobility of electrons at the 3C-SiC/SiO_2 inversion layer was developed and validated with measurements obtained from three MOS structures with dissimilar characteristics. The derived channel mobility model employs Matthiessen's rule to incorporate the influence of acoustic phonon scattering, surface roughness scattering and coulomb scattering due to fixed charges and ionized traps at the interface. The models of 3C-SiC bulk mobility (doping and field dependence) which were the subject of a previous study are also incorporated. It has been shown to predict the channel mobility for gate voltages ranging 0 – 20 V and temperatures ranging 300 – 473 K with reasonable accuracy. Since the channel region is considered an important contributor in the total resistance ($R_{DS(on)}$) of MOS-based devices, and considering the previous unavailability of appropriate 3C-SiC/SiO_2 models for TCAD simulations, this work enables more accurate and informative modelling and optimization of 3C-SiC MOS devices.

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