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The First Optimisation of a 16 kV 4H-SiC N-Type IGCT

Qinze Cao[1,a*], Peter M. Gammon[1,b], Arne Benjamin Renz[1,c], Marina Antoniou[1,d], Phil A. Mawby[1,e] and Neophytos Lophitis[2,f]

[1]School of Engineering, University of Warwick, Coventry, UK

[2]Faculty of Engineering, University of Nottingham, Nottingham, UK

[a]q.cao.2@warwick.ac.uk, [b]p.m.gammon@warwick.ac.uk, [c]arne.renz@warwick.ac.uk, [d]marina.antoniou@warwick.ac.uk, [e]P.A.Mawby@warwick.ac.uk, [f]neo.lophitis@nottingham.ac.uk

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Abstract. A challenge in the development of Silicon carbide (SiC) gate turn-off thyristors lie in an uneven transient behaviour, necessitating expensive snubbers. To address these limitations and simplify circuit topology we present an optimized 16 kV n-type SiC integrated gate commutated thyristor (IGCT) design, which utilises a novel highly doped base strip (HDBS). A particular focus is on optimizing the gate commutation of the GCT during switching, and the trade-offs in the HDBS base design were investigated. The findings reveal that compared with conventional GCT design, the HDBS design under high current conditions recorded a 11.8% reduction in turn-off power losses. When simulating the device in a high-voltage scenario, the HDBS IGCT demonstrated a 3.9% reduction in turn-off power losses and an improved turn-on power loss performance. This resulted in a reduction of power losses by 12.1% and 2.3% in high current and high voltage conditions, respectively. In summary, the novel SiC HDBS IGCT design paves the way towards a secure, high current density, and low loss switching SiC thyristor device.

Introduction

Silicon carbide (SiC) MOSFETs and diodes are now commonplace in ≤3.3kV applications, most notably in automotive inverters, thanks to the superior efficiency and switching speed they offer compared to legacy silicon (Si) IGBTs in this range. However, Si-based devices remain unchallenged in the UHV domain (>3.3kV), due in part to the processing challenges involved, the cost of large area SiC devices, and the sheer demand from the lower voltage market diverting attention. However, SiC-based thyristors have previously been demonstrated with the ability to block voltages above 15 kV whilst simultaneously scaling up current levels, suggesting they could provide an alternative to Si in applications such as future static var compensators (SVC) and in high-voltage direct current (HVDC) systems [1].

Conventional Si-based gate turn-off (GTO) thyristors have long since been constrained by their inhomogeneous transient performance, which requires costly dv/dt- and di/dt-snubbers [2-3]. In order to reduce costs and circuit topology complexity, in 1996, a novel hard-drive thyristor, referred to as integrated gate commutated thyristor (IGCT), was introduced by ABB [4].The key advantage of an IGCT compared to a conventional GTO, is its improved switching capability through commutation of the current during turn-off through the gate channel. This is achieved with the help of a dedicated gate drive unit, which averts current crowding at the cathode [5-6].

Well known as a silicon device, IGCT is entirely novel for SiC. In this work, we present for the first time an optimized design of a 16 kV n-type SiC IGCT, utilising a novel highly doped base strip (HDBS).

Methodology

An IGCT consists of three components: a clamping circuit, a gate-drive circuit, and the gate commutate thyristor (GCT) device. In this paper, our focus will be primarily on optimizing the GCT device itself. The optimised structures of a conventional GCT design and a GCT with a HDBS are

shown in Fig. 1. In both cases, a 2 µm thick, 5×10^{17} cm^{-3} N-field stop layer is grown on top of a 15 µm thick, 1×10^{19} cm^{-3} P-type injector which serves as the anode of the IGCT. A 160 µm, 2×10^{14} cm^{-3} drift region is used to support the 16kV bias during off state. During the simulation, the P-base layers were varied to optimise the performance. The cathode is 2 µm thick with a doping concentration of 1×10^{19} cm^{-3}. The distance between the cathode edge and gate is fixed at 5 µm to aid manufacturing. The gate width is 10 µm.

Throughout the entire investigation, Synopsys TCAD was deployed using benchmarked physics models including Shockley-Read-Hall, Auger and Avalanche Okuto Crowell model in recombination, Incomplete Ionization, thermodynamic, etc [7]. The carrier lifetime was set to either 2 µs or 10 µs for static and transient simulations respectively. Room temperature (300k) is used for all the simulation. A double pulse test circuit, shown in Fig. 2, was employed for transient simulations. With this setup, the trade-offs that dictate the IGCT characteristics (blocking voltage, on state loss, fast turn-off capability and turn-on time) were investigated. In the end, the impact of the HDBS base design was investigated.

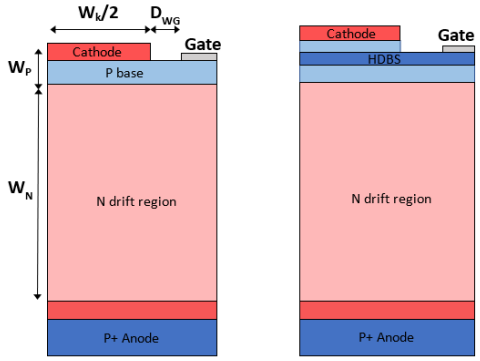

Fig. 1. Cross-sections of left, a conventional GCT; and right, the GCT with HDBS.

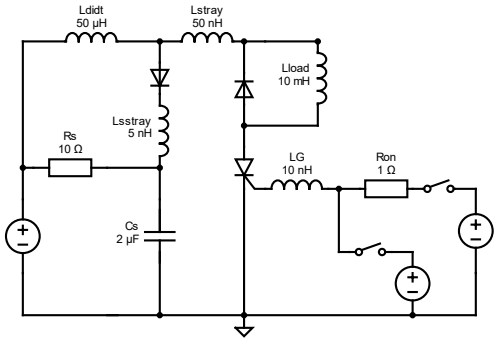

Fig. 2. Schematic of the double pulse circuit with clamping circuit, turn-on voltage = 5V, turn-off voltage = -100V when V_{dd}=5000V, J_{ak}=190A/cm^2; or turn-off voltage = -20V when V_{dd}=15000V, J_{ak}=30A/cm^2

Simulation Results and Discussion

For the conventional GCT, the impact of base width (W_P) and p-base doping was investigated at the beginning. An increase of either increases the forward voltage drop (Fig. 3) but improves the IGCT switching speed (Fig. 4). This is thought be due to reduced electron injection across the p-base. For optimisation purposes, a 2 µm thick p-base layer with doping of 1×10^{17} cm^{-3} was selected for the conventional device. In the HDBS device, the total dose was kept similar to isolate the effect of the HDBS layout. Therefore, the HDBS base design comprises a 1 µm thick and 2×10^{17} cm^{-3} doped layer, sandwiched between two lightly doped regions of 1×10^{15} cm^3 doping, 1 µm (above) and 2 µm (below) thick. The resulting 1.5% increase of total dose is reflected in the Fig. 5, where the forward voltage drop of the HDBS is consistently 1.5% higher than the conventional design. Fig. 5 depicts the trade-off between on-state performance of the conventional device and half-cell cathode width ($W_K/2$). It also reflects the ratio between cathode and the 10 µm of non-cathode top surface, from the centre of the gate to the cathode edge. The obtained penalty is an increase in switching losses, shown in Fig. 6, as a wider cathode results in a longer commutation path during switching. A half-cell cathode width of 47 µm was chosen for the rest of the simulations, as there are negligible on-state advantages above this value.

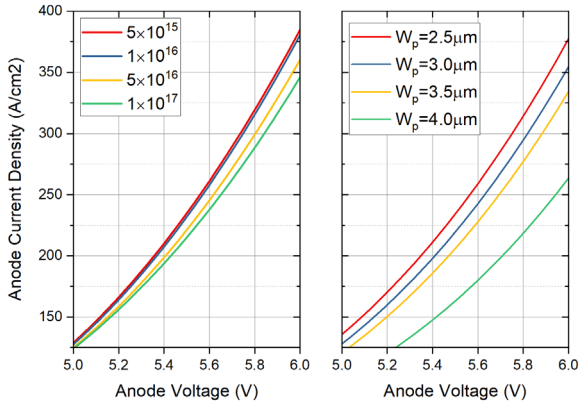

Fig. 3. Anode current over anode voltage of a conventional GCT design varying (left) the P base doping, and (right) the P base length.

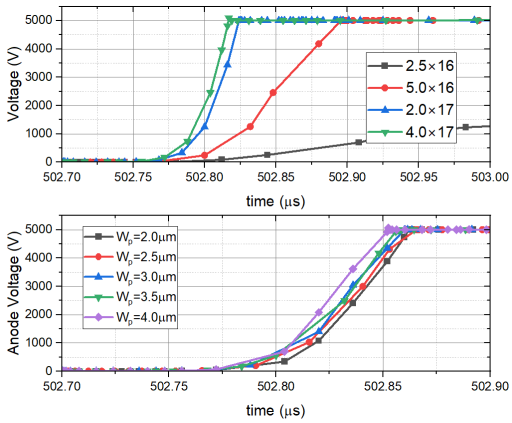

Fig. 4. Voltage waveforms of a conventional GCT design during turning-off, varying the P base doping (top), and the P base length (bottom).

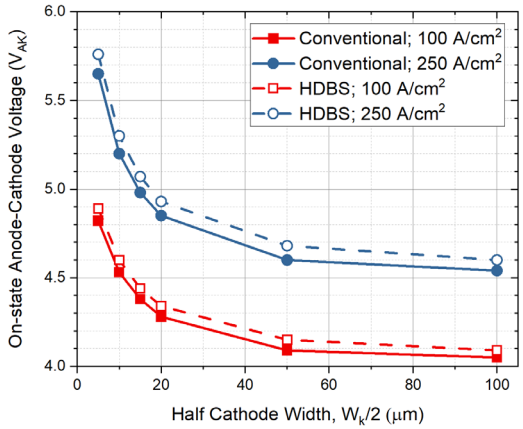

Fig. 5. Forward voltage drop of the conventional IGCT design and the HDBS design at 100 and 250 A/cm^2 for different $W_k/2$. Gate width was fixed at 5 µm.

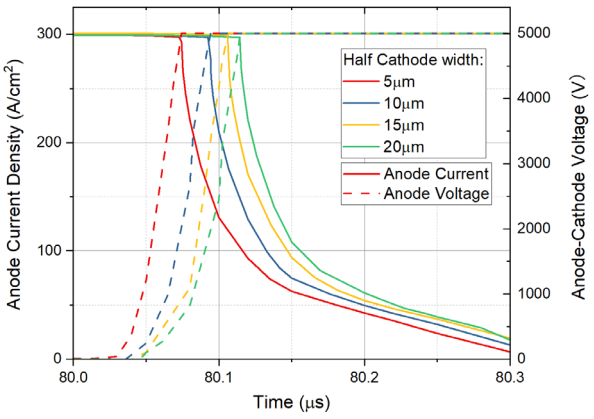

Fig. 6. Turn off performance of a conventional GCT design with cathode widths (W_k) varying from 5 to 20 µm, for a constant gate width of 5 µm, p-base doping of 1×10^{17} cm^{-3}, base length of 2 µm, and a gate reverse bias of 100V.

Two switching conditions were considered: Fig.7 shows the anode and gate turn-off characteristics of the two devices, compared under high current conditions; Fig. 8 shows the same under high voltage conditions. Under high current conditions, the HDBS structure has 11.8% less turn-off power losses (derived from Fig. 7). This is visualised in Fig. 9 (left) where, in the conventional GCT, a highly current dense filament can be seen crossing the base to the cathode while a depletion region is forming in the drift region at 503 µs, because the high p-base resistance and commutated current forming a voltage difference between the cathode centre and the gate, this voltage difference cancels out with the gate voltage, preventing the commutation of current along the full length of the base region. Conversely, in Fig. 9 (right) the HDBS provides a lower resistance path through the p-base, and hence the depletion region formed at the base-cathode interface traverses the full width of the cathode, which transforms the original GTO turning-off process into an open-base PNP transistor switching off. Under high voltage (low current) conditions, the turn-off power loss advantage of the HDBS IGCT is 3.9% compared to the conventional IGCT.

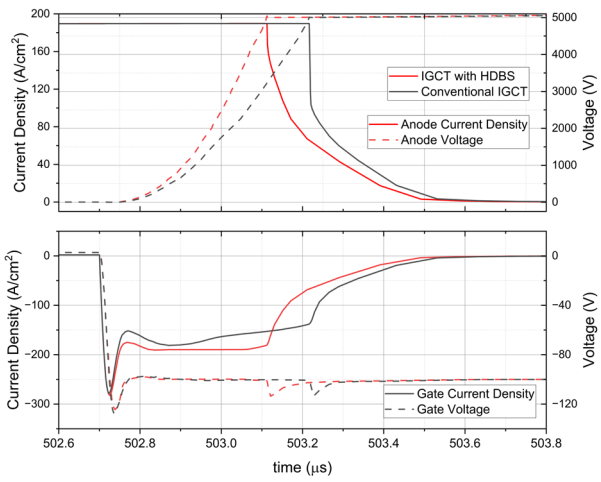

Fig. 7. IGCT turn-off switching characteristics in high current conditions. The on state current density J_a is 190Acm^{-2}, the turn-off Vg is -100V and the V_{dc} is 5kV. Turn-off losses are 197.4mJ and 223.9mJ for IGCT with HDBS and conventional IGCT.

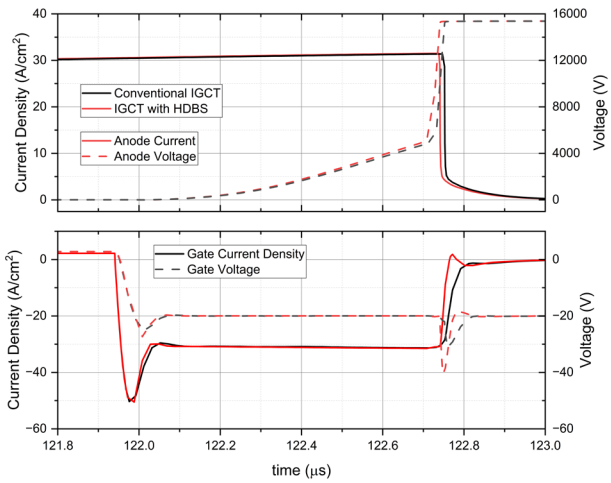

Fig. 8. IGCT turn-off switching characteristics in high voltage conditions. The on state current density J_a is 30Acm^{-2}, the turn-off Vg is -20V and the V_{dc} is 15kV. Turn-off losses are 77.1mJ and 80.2mJ for IGCT with HDBS and conventional IGCT.

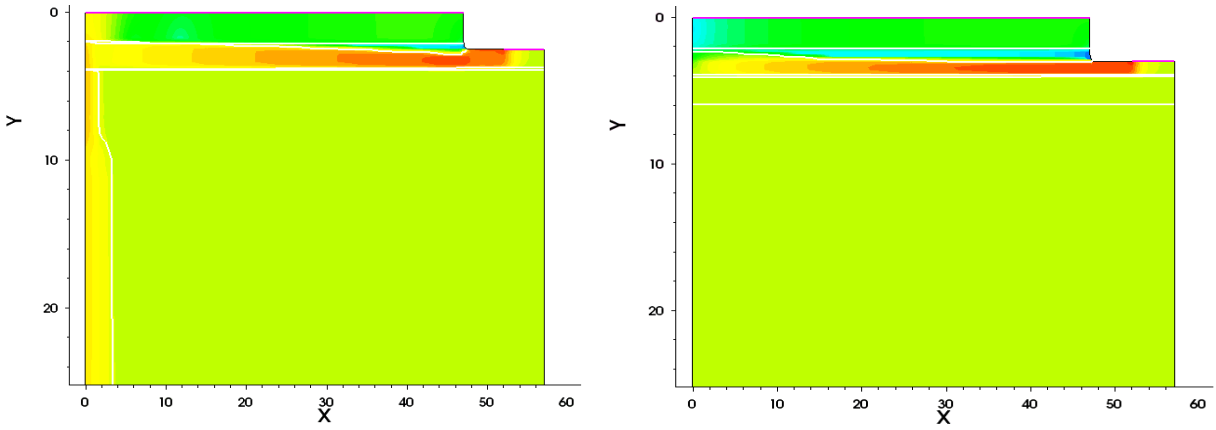

Fig. 9. Current density distribution in the cathode-base-drift regions of a conventional (left) and HDBS (right) GCT.

The anode and gate turn-on characteristics of the two devices under high current and high voltage conditions are shown in Fig. 10 and 11 respectively. The HDBS IGCT improves the turn-on power loss also performance also, by 9.4% and 2.3% compared to the conventional IGCT in high current and high voltage conditions. This is because HDBS facilitates the lateral diffusion of the injected gate current within the P-base region. The lateral spreading velocity is directly proportional to anode di/dt during turn on [8], resulting in a reduction in turn-on time and power loss.

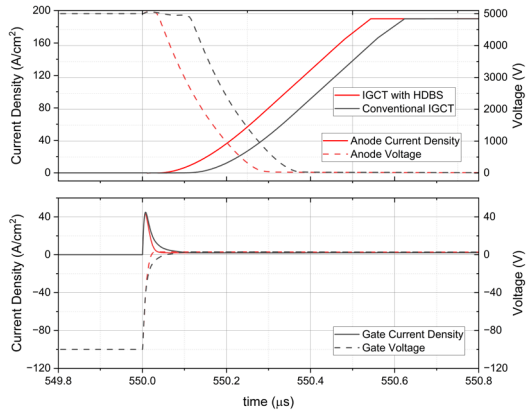

Fig. 10. IGCT turn-on switching characteristics in high current conditions. The on state current density J_a is 190Acm^{-2}, the turn-on Vg is 5V and the V_{dc} is 5kV. Turn-on losses are 5.91mJ and 6.52mJ for IGCT with HDBS and conventional IGCT.

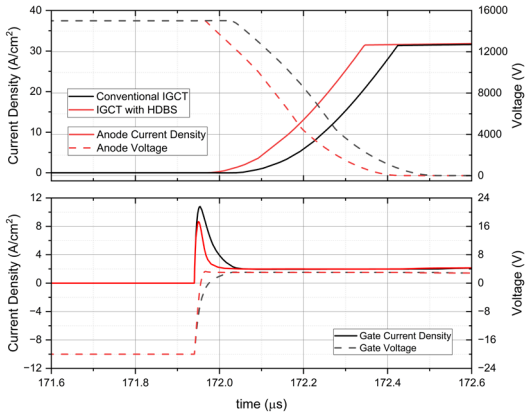

Fig. 11. IGCT turn-on switching characteristics in high voltage conditions. The on state current density J_a is 30Acm^{-2}, the turn-on Vg is 5V and the V_{dc} is 15kV. Turn-on losses are 15.5mJ and 15.9mJ for IGCT with HDBS and conventional IGCT.

Summary

This study delved into the optimization of Silicon carbide (SiC)-based thyristors, particularly focusing on the integrated gate commutated thyristor (IGCT) for SiC. Our research presented an optimized design of a 16 kV n-type SiC IGCT, leveraging a novel highly doped base strip (HDBS). Through comprehensive simulations using Synopsys TCAD, we investigated the trade-offs influencing IGCT characteristics and the subsequent impact of the HDBS base design. The results highlighted the advantages of the HDBS design, particularly in reducing turn-off power losses by 11.8% under high current conditions and 3.9% under high voltage conditions. Furthermore, the HDBS IGCT showcased improved turn-on power loss performance by 9.3% and 2.3% in high current and high voltage scenarios, respectively. The HDBS's ability to facilitate lateral diffusion of the injected gate current within the P-base region was instrumental in this improvement. In conclusion, the SiC HDBS IGCT design offers a promising avenue towards a secure, high current density, and efficient switching thyristor, marking a significant advancement in thyristor technology, paving the way for more efficient and cost-effective high-power electronic systems in the future.

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