3C-SiC-on-Si MOSFETs: Overcoming Material Technology Limitations

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***Abstract*—The cubic polytype (3C-) of silicon carbide (SiC) is an emerging semiconductor technology for power devices. The featured isotropic material properties along with the wide band gap characteristics make it an excellent choice for power metal oxide semiconductor field effect transistors (MOSFETs). It can be grown on silicon (Si) substrates which is itself advantageous. However, the allowable annealing temperature is limited by the melting temperature of Si. Hence, devices making use of 3C-SiC on Si substrate technology suffer from poor or even almost negligible activation of the p-type dopants after ion implantation due to the relatively low allowable annealing temperature. In this article, a novel process flow for a vertical 3C-SiC-on-Si MOSFET is presented to overcome the difficulties that currently exist in obtaining a p-body region through implantation. The proposed design has been accurately simulated with technology computer-aided design process and device software. To ensure reliable prediction, a previously validated set of material models has been used. Further, a channel mobility physics model was developed and validated against experimental data. The output characteristics of the proposed device demonstrated promising performance, what is potentially the solution needed and a huge step toward the realization of 3C-SiC-on-Si MOSFETs with commercially grated characteristics.**

***Index Terms*—3C-SiC-on-Si, MOSFETs, silicon carbide, stopping and range of ions in matter (SRIM), technology computer-aided design (TCAD), wide band gap.**

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I. Introduction

SILICON carbide (SiC) is a wide band gap (WBG) semiconductor material with superior material characteristics compared to silicon (Si). Due to that, devices based on this material are expected to replace their Si counterparts in power electronic applications. These WBG properties include at least two times wider energy bandgap, an order of magnitude higher critical electric field (Ecr), and largely improved thermal conductivity. SiC can be polymerized in numerous polytypes, nonetheless only one cubic (3C-) phase of SiC exists. The isotropic characteristics of 3C-SiC [1], [2] in conjunction to its remarkable thermal conductivity makes it a prime option for WBG power devices. The cubic SiC can be heteroepitaxially grown on Si substrates using chemical vapor deposition (CVD) [3]. This enables for large 3C-SiC-on-Si crystals that match the diameters of commercially available Si wafers [4]. In consequence, discrete power devices of reduced cost can be obtained. Furthermore, the interest in the monolithic integration of SiC devices with Si technology makes the 3C-SiC an excellent WBG semiconductor for power devices.

The 3C-SiC is particularly promising for metal oxide semiconductor field effect transistors (MOSFET)s, in spite of its smaller bandgap compared to the two other major hexagonal SiC polytypes (4H-, 6H-) [5]. Indeed, it has been shown that a 3C-SiC MOS-based switch can achieve less switching losses compared to a 4H-SiC MOS-based switch with the same blocking capabilities [6]. Further, its smaller critical electric field value is beneficial for high frequency MOSFETs [7]. Notably, due to the narrower bandgap energy window of 3C-SiC, the majority of the observed SiO_2/SiC interface traps are energetically located in the conduction band (E_C), essentially improving the effective channel mobility [8–11].

Both vertical and lateral 3C-SiC-on-Si power MOSFETs have been developed and characterized in the literature [12–17]. However, they are not commercialized yet because of the high planar defects density in the 3C-SiC-grown layers originating from the heterointerface to Si during growth [18]. Currently, this is the main bottleneck for the 3C-SiC-on-Si material technology that hinders its anticipated device performance potential.

It has been demonstrated that the density of the SiO_2/3C-SiC-on-Si interface states (D_{it}) heavily depends on the quality of the initial epilayer [19]. The volume of the formed planar defects can be reduced when 3C-SiC is grown on undulant-Si substrates [4]. In [5], Metal oxide semiconductor (MOS)

capacitors fabricated on a 3C-SiC-on-Si surface after ultraviolet (UV) irradiation/ozone cleaning had their SiO_2/SiC interface properties greatly improved. It is also reported that a shallow nitrogen (N) implantation at the gate oxide region prior to the thermal oxidation reduces the D_{it} [20]. Therefore, improvements of the 3C-SiC heteroepitaxy set the premises on delivering significantly more reliable MOS structures.

Interestingly, one of the 3C-SiC beneficial properties, the ability to grow on cheap and large diameter Si substrates, also raises another challenge for this technology in terms of p-type doping. Boron (B) and aluminum (Al) are two of the most preferable p-type dopants for 3C-SiC. However, the B is linked with the formation of deep energy levels in the SiC [21]. At the same time, the physical similarities of Al and Si in terms of atomic size and masses prevent lattice distortions that can act as scattering centers. Thus, Al is the main option for planar selective area doping for the formation of p-type region in the 3C-SiC material.

The Si substrate limits the activation temperature of the acceptor-type implanted dopants in 3C-SiC below its melting point. This value of approximately 1412 °C [22] is further down compared to the required annealing temperatures of Al, which can be as high as 1700 °C for a nearly perfect activation (>95%) [23]. In consequence, p-type regions by ion implantation are difficult to achieve.

The challenging nature of acceptor activation is also highlighted in [24], where 3C-SiC samples implanted at 850 °C and annealed at 1200 °C demonstrated n-type electrical behavior. P-type behavior was only observed when the sample was annealed at 1400 °C. Similarly, measurements in [25] demonstrated an activation level for the dopants of less than 1%. Such inefficient holes' generation process demands high acceptor dopant concentration for p-type 3C-SiC, which in turn induces more lattice defects deteriorating the hole mobility. This challenge can be a limiting factor for conventional 3C-SiC-on-Si MOSFET designs.

In this article, a novel process flow is proposed for the fabrication of vertical 3C-SiC-on-Si MOSFETs which eliminates the need for Al implantation. This includes a homoepitaxially grown p-layer on top of the n-drift layer, rather than formatting the p-body with multiple implants. The proposed design has been developed with the technology computer-aided design (TCAD) synopsys process tool and its performance simulated with synopsys device tool. A previously validated set of physics models are used to accurately describe the 3C-SiC material which was previously published in [26], [27]. Traps at the interface between SiO_2/3C-SiC have also been included with density values that agree with reported fabricated structures in the literature for this technology. The results in this work highlight that the proposed design is able to deliver 3C-SiC-on-Si MOSFETs with excellent output characteristics.

II. Novel MOSFET Design and Fabrication Method

The viability of the conventional implanted body design method, in Fig. 1, is under question for 3C-SiC-on-Si MOSFETs because of the reported challenges in the activation of p-type dopants in cubic SiC polytype [24], [25]. In an effort to address this major material-related issue, an alternative MOSFET design and fabrication methodology is proposed. Instead of forming the p-body regions by implantation, it is proposed to grow a thin 3C-SiC layer of p-type conductivity on top of the heteroepitaxially grown n-drift 3C-SiC layer. This can be achieved by changing the SiC epitaxial film growth conditions in the chamber from N- to Al-rich environment. Thereafter, the JFET region can be shaped with implants of high N concentration to overcompensate the desired areas. Implanted N in 3C-SiC-on-Si is known to activate at low annealing temperature, which makes this a viable alternative fabrication process. Due to the resulting highly doped regions, such device cannot block significant voltage and can break prematurely. The proposed design includes novel features shown in Fig. 1, which allow the mitigation from high concentration of electric fields. With the application of appropriate masks, a localized super-junction (S-J) is created in the form of edges extending from the body into the JFET region. They assist in largely mitigating the charge imbalance and maintaining high blocking voltage capability.

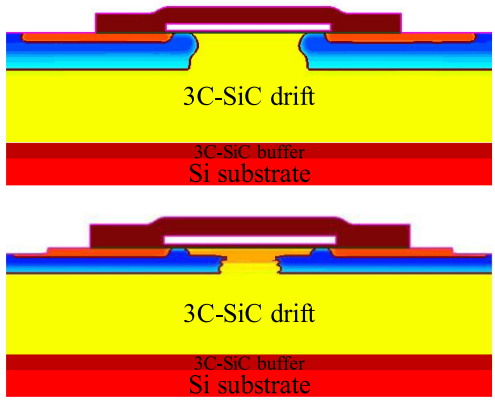

Fig. 1. Conventional implanted body MOSFET design (top) and the novel S-J JFET MOSFET design (bottom).

A. Epitaxially Grown P-Body Region

The proposed 3C-SiC-on-Si MOSFET with S-J JFET region suggests homoepitaxy of a thin 3C-SiC layer of p-type conductivity on top of the heteroepitaxially grown n-drift 3C-SiC layer. Two variants of the *in situ*-doped p-body region are investigated, one with gradual doping profile and another one with stepped profile.

The stepped doping profile comprises of four doping levels, which exist one after another following a step-wise pattern, as illustrated with the dashed horizontal lines in Fig. 2. Beginning from the 3C-SiC surface and expanding up to a depth of 0.15 μm, a constant doping level of $N_A = 5 \times 10^{16}\text{cm}^{-3}$ is considered. Following, the second step is a constant doping level of $N_A = 1 \times 10^{18}\text{cm}^{-3}$ characterizing the region from 0.15 up to 0.45 μm. The third doping step of $N_A = 1 \times 10^{17}\text{cm}^{-3}$ is valid up to a depth of 0.575 μm from the semiconductor surface and then the fourth doping level of $N_A = 8 \times 10^{15}\text{cm}^{-3}$ completes the stepped doping profile in the p-body at the depth value of 0.7 μm.

The gradual doping profile is obtained by altering gradually the concentration of acceptors during the epitaxial growth

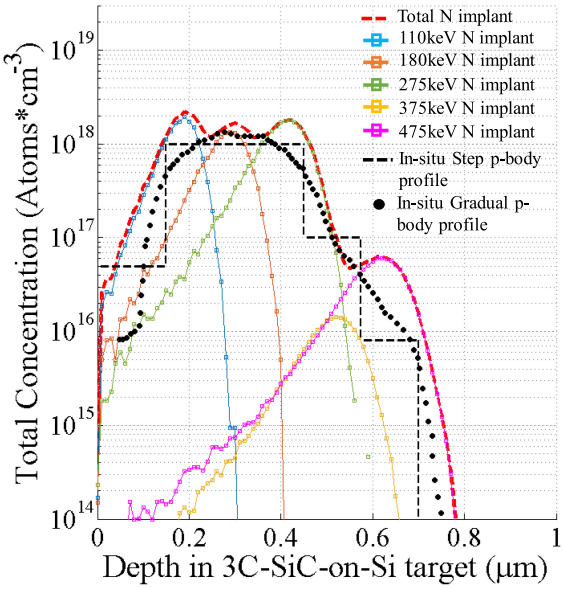

Fig. 2. The *in situ* doping profiles of the p-body (both gradual and step-wise) and the total N implanted for the n-JFET overcompensation.

process. The gradual doping profile is illustrated with filled circular marks in Fig. 2.

Both the stepped and the gradual profiles were designed to be comparable and similar. Importantly, they feature a retrograde profile. The p-body doping at the 3C-SiC surface is designed with low concentration, in the range of $1-5\times10^{16}\mathrm{cm}^{-3}$, to increase the controllability of the threshold voltage value within 3–5 V. The p-body doping concentration increases with increasing depth until a peak value is reached and then drops to a minimum merit. The peak concentration needs to be high enough ($\sim1\times10^{18}$) to support high voltage and avoid punchthrough.

B. Implanted JFET Region

The n-type JFET is formed with several N ion implantation of adequate levels to overcompensate the doping of the p-body. The minimum steps of N implants required to form the JFET, along with the corresponding implantation energies, were determined with accurate Monte–Carlo simulations, utilizing the stopping and range of ions in matter (SRIM)/transport of ions in matter (TRIM) model for 3C-SiC target material [28]. For each independent implantation step simulated on the 3C-SiC target material, the obtained nitrogen fluence Gaussian distribution was interpolated to a common penetration depth-axis. The combination of five implant steps with energies 110, 180, 275, 375, and 475 keV was established, resulting in a doping profile with the capacity to adequately overcompensate the p-body doping for the desired depth. Considering sufficient dose values, as listed in Table I, the predicted net profile from the implanted N is illustrated in Fig. 2, co-plotted with the *in situ* gradual and stepped doping profiles within the p-body.

C. Super-Junction JFET Region

The precise compensation of the homoepitaxially grown p-body layer is a challenging task. To ensure overcompensation

TABLE I
DOSE VALUES FOR THE N IMPLANTS TO FORM THE N JFET DOPING PROFILE IN FIG. 2 BASED ON SRIM/TRIM SIMULATIONS

Target/Ion	Implant Energy (keV)	Peak Fluence (cm^{-3})/(cm^{-2})	Dose (cm^{-2})
3C-SiC/N	110	$1.17x10^{5}$	$1.7x10^{13}$
3C-SiC/N	180	$9.05x10^{4}$	$1.5x10^{13}$
3C-SiC/N	275	$7.86x10^{4}$	$2.3x10^{13}$
3C-SiC/N	375	$7.14x10^{4}$	$2.0x10^{11}$
3C-SiC/N	475	$6.81x10^{4}$	$9.0x10^{11}$

and the successful formation of an n-type conductivity continuous JFET region, the doses of each N implant should generate a concentration higher than the underlying concentration of holes. To overcompensate the highly doped p-body layers, the obtained JFET is, in turn, also highly doped. This has the potential of reducing the ON-resistance ($R_{\mathrm{DS,on}}$) at the expense of blocking voltage degradation. To counterbalance the loss of blocking ability, the implantation of N is carried out through masks to form an S-J region. The proposed process, in Fig. 3, leads to the formation of edge-shaped p-type regions within the JFET, resulting in S-J JFET designs. The process steps for the proposed S-J JFET design comprise (a) *in situ* growth of the p-body layer on the 3C-SiC-on-Si n-drift, (b1) application of a first mask for ion implantations up to 275 keV, from Table I, to form the first stage of the n-JFET, (b2) application of an additional mask to spatially limit the higher energy implants [29], (c) ion implantation to form the n-source pads, and (d) etching of the lowly doped surface of the p-body to reach the high concentration part of p-body. This helps suppressing the parasitic bipolar junction transistor (BJT), (e) oxidation for the gate oxide formation, (f) deposition of gate metal, (g) oxide deposition as an interlayer dielectric (ILD) to isolate gate and source conductors from each other, (h) opening of the source contacts, and (i) source metallization.

III. THE IMPLANTED BODY 3C-SIC-ON-SI MOSFET DESIGN

Although the real activation of acceptor-type implants in 3C-SiC-on-Si is minimal, a TCAD model of such conventional MOSFET can be tuned to have equivalent activation to that of *in situ* acceptor doping. The finite element analysis (FEA) simulation results for this theoretical MOSFET design can be used as reference for the direct comparison of the proposed MOSFET with S-J JFET. They also constitute the theoretical performance limit.

To create the theoretical 3C-SiC-on-Si MOSFET model according to the implanted body design method, the sProcess TCAD tool is utilized. The moderately doped n-drift layer is obtained with heteroepitaxy on an isotype Si substrate. The p-body region is formed by selective ion implantations to result in a doping profile similar to the one considered for the proposed S-J JFET designs. The net implanted profile for the p-body considering all the Al implants, as predicted by SRIM/TRIM, is illustrated in Fig. 4. The terms conventional and implanted body design method will be used interchangeably for the rest of this work.

The detailed process steps for the proposed implanted body MOSFET design comprise (a) ion implantation to form the p-body

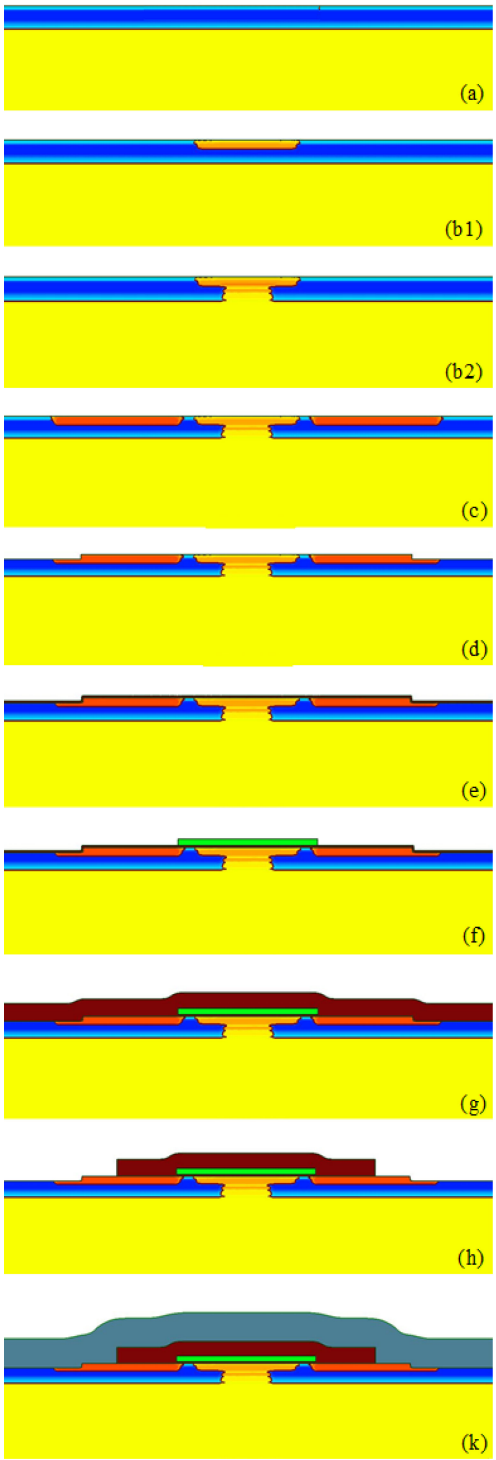

Fig. 3. Fabrication process for novel vertical MOSFET featuring S-J JFET.

with the doping profile illustrated in Fig. 4, (b) additional Al implants at the source contact sides to reduce the possibility of parasitic BJT latch-up, (c) ion implantation to form the n-source pads, (d) oxidation for the gate oxide, (e) deposition of gate metal, (f) oxide deposition as an ILD to isolate gate and source conductors from each other, (g) opening of the source contacts, and (h) source metallization. Simulating these process steps, the resulted implanted body MOSFET is shown in Fig. 1.

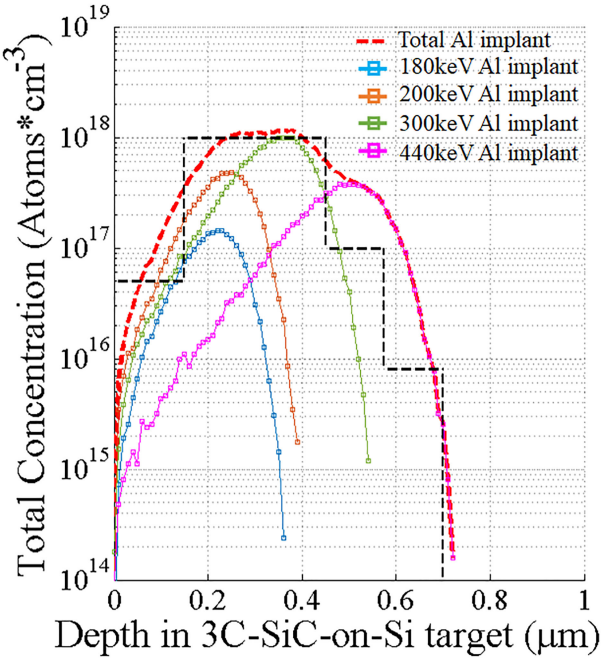

Fig. 4. The total Al implants considered for the implanted body of a conventional 3C-SiC-on-Si MOSFET design.

IV. Experimentally Validated Channel and Accumulation Layer Mobility Model for 3C-SiC MOS Structures

To analyze the proposed MOSFET, it is important to use models which can replicate the physical phenomena taking place within the device. The degradation of mobility at the $3C-SiC/SiO_2$ interface due to electron–phonon scattering effects is of particular importance for MOSFET performance analysis. In this section, an appropriate model is presented and validated against experimental measurements. In the inversion layer of a SiC MOSFET, the high transverse electric field forces electrons to interact strongly with the SiC-insulator interface. In turn, the channel region is considered to be among the regions that contribute the most to the resulted device ON-state resistance.

According to the Matthiessen's rule (1), the mobility of the carriers within an n-type channel ($\mu_{\rm ch}$) results as a weighted degradation contribution due to doping level ($\mu_{\rm dop}^{\rm 3C-SiC}$), electric field ($\mu_{E//}^{\rm 3C-SiC}$), and scattering phenomena. Both the $\mu_{\rm dop}^{\rm 3C-SiC}$ and the $\mu_{E//}^{\rm 3C-SiC}$ have been accurately modeled in previous works by the authors of this article [26], [27]. In particular, the $\mu_{E//}^{\rm 3C-SiC}$ degradation component is due to the electric field element parallel to the current flow. On the contrary, the transverse electric field ($\mu_{E^{\perp}}$) is the driving force for the mobility degradation due to scattering at the semiconductor/oxide interface. The latter comprises acoustic phonon scattering ($\mu_{\rm ac}^{\rm 3C-SiC}$), surface roughness scattering ($\mu_{\rm SR}^{\rm 3C-SiC}$), and Coulomb scattering with charged traps and fixed charges ($\mu_{\rm cb}^{\rm 3C-SiC}$). In Matthiessen's rule, to switch OFF the inversion layer terms far away from the interface, the damping parameter $D =$

$\exp(-x/l_{\text{crit}})$ is deployed, where x is the actual distance from the interface.

$$\mu_{\text{ch}} = \frac{1}{\mu_{\text{dop}}} + \frac{1}{\mu_{E//}} + \frac{D}{\mu_{\text{ac}}} + \frac{D}{\mu_{\text{SR}}} + \frac{1}{\mu_{\text{cb}}} \tag{1}$$

$$\mu_{\text{ac}} = \frac{B}{E_{\perp}} + \frac{CN_A^{\lambda}}{E_{\perp}^{1/3}(T/300)^{k_1}} \tag{2}$$

$$\mu_{\text{SR}} = \left(\frac{E_{\perp}^{A^*}}{\delta} + \frac{E_{\perp}^3}{\eta}\right)^{-1} \tag{3}$$

$$A^* = A_{\text{init}} + \frac{(a_{\perp,n}n + a_{\perp,p}p)\, N_{\text{ref}}^{\beta}}{N_A^{\beta}} \tag{4}$$

$$\mu_{\text{cb}} = \frac{\mu_1 \left(\frac{T}{300}\right)^{k_2} \left\{1 + \left[n/\left(n_{\text{trans}}\left(\frac{D_i}{N_0}\right)^{\eta_1}\right)\right]^{\upsilon}\right\}}{\left(\frac{D_i}{N_0}\right)^{\eta_2} e^{-d_{\text{int}}/l_{\text{crit}}} \cdot \left(1 - e^{-(E_{\perp}/E_0)^{\gamma}}\right)}. \tag{5}$$

The model developed for the degradation of electrons' mobility at the 3C-SiC/SiO_2 inversion layer due to scattering according to (2)–(5) has been validated utilizing channel mobility measurements obtained from a 3C-SiC n-MOS structure featuring poly-Si as gate metal, $t_{\text{ox}} = 64$ nm of SiO_2 gate oxide and a characterized $D_{it}^{3\text{C}-\text{SiC}} = 1.8 \times 10^{12}\text{cm}^{-2}$, whilst the p-body doping has been assessed $N_A = 2.5 \times 10^{17}\text{cm}^{-3}$ [30]. The geometry of this 3C-SiC n-MOS structure was accurately replicated with TCAD ensuring a fine meshing for the inversion layer. The channel was considered within 1–5 nm from the interface between the 3C-SiC and the SiO_2 and is delimited by the parameter value l_{crit}. Considering $T = 300$ K, the driving forces ($E_{\perp}$, $E//$) and the densities of both free electrons (n) and free holes (p) at the channel region were extracted from the simulated structure and imported in MATLAB allowing a complex mathematical correlation of the parameters for (2)–(5) resulting in the values presented in Table II.

Since operation at elevated temperatures is a key feature of SiC devices, the developed model was expanded to predict the dependency on temperature. This dependency is described with the parameters k_1 and k_2, in (2) and (5) correspondingly, the values of which were determined utilizing channel mobility measurements at $T = 473$ K from the same n-MOS structure [30].

In Fig. 5, the incorporation of the developed model in the Matthiessen's rule (1) is capable of reproducing the measured channel mobility values as both a function of the applied gate voltage and temperature.

TABLE II
VALIDATED PARAMETER VALUES FOR THE CHANNEL MOBILITY IN 3C-SIC MOS DEVICE CONCEPTS

Parameter	Scattering Type	Value
$B\ (cm \cdot s^{-1})$	(2)	$5x10^{8}$
$C(cm^{5/3}V^{-2/3}s^{-1})$	(2)	$5x10^{2}$
λ	(2)	0.1
k_1	(2)	5
$\delta(cm^2V^{-1}s^{-1})$	(3)	$5x10^{16}$
$\eta(V^2cm^{-1}s^{-1})$	(3)	$3x10^{20}$
A_{init}	(4)	2.1
$\alpha_{\perp,n}(cm^3)$	(4)	$6.85x10^{-21}$
$\alpha_{\perp,p}(cm^3)$	(4)	
$N_{ref}(cm^{-3})$	(4)	1
β	(4)	$92x10^{-3}$
$E_0(Vcm^{-1})$	(5)	$1x10^{-6}$
$N_0(cm^{-2})$	(5)	$1x10^{11}$
γ	(5)	1
$\mu_1(cm^2V^{-1}s^{-1})$	(5)	1
$n_{trans}(cm^{-3})$	(5)	$2x10^{16}$
η_1	(5)	0.1
η_2	(5)	0.4
υ	(5)	1.2
$d_{int}(cm)$	(5)	$5x10^{-8}$
$l_{crit}(cm)$	(5)	$7x10^{-7}$
k_2	(5)	1.5

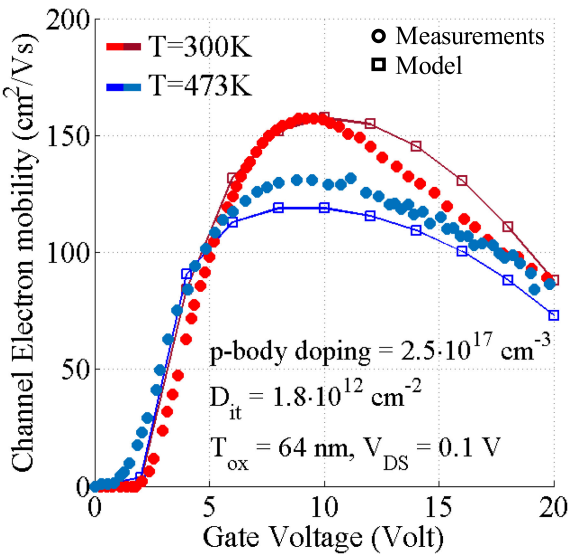

Fig. 5. Developed channel mobility model is capable of predicting the measurements obtained from the 3C-SiC n-MOS structure [30] for a wide range of gate voltage values and for different temperatures.

V. EVALUATION OF THE PROPOSED S-J JFET 3C-SIC-ON-SI MOSFET DESIGN

Synopsys Sentaurus Device (sDevice) [31] tool has been used to simulate the electrical performance of the proposed structures (Fig. 3). Key to these simulations is the utilization of a previously developed and validated material model for bulk 3C-SiC material [21], [27]. The sProcess MOS-structures, both the S-J JFET and the implanted body designs, feature a cell pitch of 16 μm, whilst the drift layer is modeled 10 μm thick and $5 \times 10^{15}\text{cm}^{-3}$ n-type doped. A highly doped buffer layer is also considered of 1 μm thickness between the 3C-SiC drift and the Si substrate. The latter is assumed to be 110 μm thick and $1 \times 10^{19}\text{cm}^{-3}$ N doped. The source n+ regions are highly doped to ensure good ohmic contacts. Moreover, positive fixed charges are modeled at the 3C$-$SiC/SiO_2 interface with $D_{\text{it}}^{3\text{C}-\text{SiC}} = 2.5 \times 10^{11}\text{cm}^{-2}$, in accordance with characterized values from the literature [5], [17].

The geometries of the simulated MOS systems were aimed to be identical, enabling a direct comparison of their electrical performance. Regarding the MOS interface, all the considered

designs feature the same $D_{\rm it}^{\rm 3C-SiC}$ and a gate oxide thickness of $t_{\rm ox} = 60$ nm. The doping profiles in the body region, for both the *in situ* (Fig. 2) and the ion-implanted (Fig. 4) cases, are designated to be similar. In consequence, the implanted body and the edge S-J JFET-simulated devices exhibited a threshold voltage value in the range of $V_{\rm th} = 3.2 - 3.7$ V. The active area of the devices considered for this work is 7.3×10^{-4} cm^2 and it is equivalent to the fabricated 3C-SiC MOSFET in [14].

A. Charge Imbalance

To evaluate and optimize the suggested 3C-SiC-on-Si MOSFET design featuring S-J JFET, a thorough simulation study was carried out. The doses of each N implant step, in Fig. 2, were varied while keeping the implant energies fixed. Each time, the values of all the doses were modified in like manner, i.e., as a percentage of the initial dose values considered in Table I, to determine a new design variant for simulation. This resulted in MOSFET designs with different amount of charge within the formed S-J JFET.

The higher the dose values, the more the stored charge in the S-J regions, deteriorating the blocking capability of the body diode. Given that the charge at the p-type regions of the S-J (Q_p^{S-J}) is constant (placed *in situ*), modifying the charge of the n-type S-J JFET (Q_n^{S-J}) essentially alters the charge balance of the body diode. This charge imbalance is critical for the performance of the proposed MOSFETs in the forward blocking mode. In consequence, the charge imbalance formula in (6) is utilized to investigate the effect of the stored charge at the n-JFET on the breakdown voltage.

$$\text{Charge imbalance } (\%) = \frac{Q_p^{S-J} - Q_n^{S-J}}{Q_p^{S-J}} \times 100. \quad (6)$$

The stored charge in the p $-$ (Q_p^{S-J}) and n-type (Q_n^{S-J}) S-J parts is calculated for each simulated design variant by integrating the concentration of the corresponding activated dopants up to the desired depth, i.e., the depth of the JFET region, and then multiplying the outcome with the width of the region of interest. For the edge S-J JFET designs, the calculation for the charge in the n-JFET splits in two parts, that is one for the upper and one for the bottom JFET region. The left and right edges are accounted for the p-type charge of the S-J.

The defined trade-off between the calculated charge imbalance (6) and the breakdown voltage, after handling the dose of each implant as variable, is shown in Fig. 6 for the proposed S-J JFET MOSFET. A transition on the x-axis from right to left indicates increased dose values for the N implants resulting in a more negative charge imbalance value. A fitting curve is co-plotted in Fig. 6, to illustrate the predicted behavior, suggesting a safe window from -65% up to 0% for the edge S-J design for a targeted $V_{\rm BR} > 500$ V. Notably, when the charge imbalance curve, in Fig. 6, approaches the 0% point, the overcompensation of the p-body is less likely to be complete. In such undesired cases, p-stripes exist in the JFET, which obstruct the free electron flow, resulting in a non-MOSFET structure characterized by an excessive resistance value.

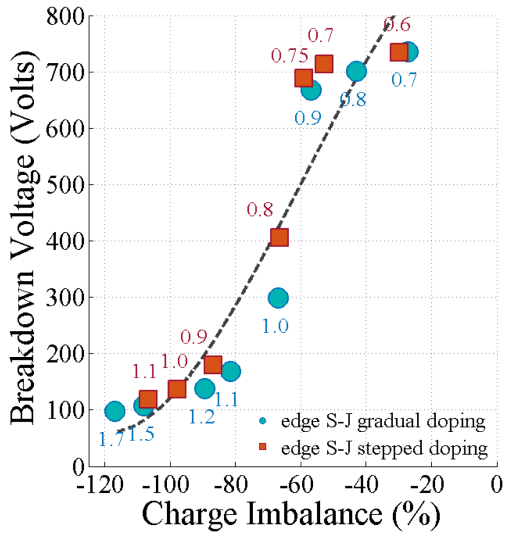

Fig. 6. Blocking voltage as a function of the charge imbalance for the simulated devices. The points annotation correspond to the percentage of the dose values listed in Table I considered for the particular design variant.

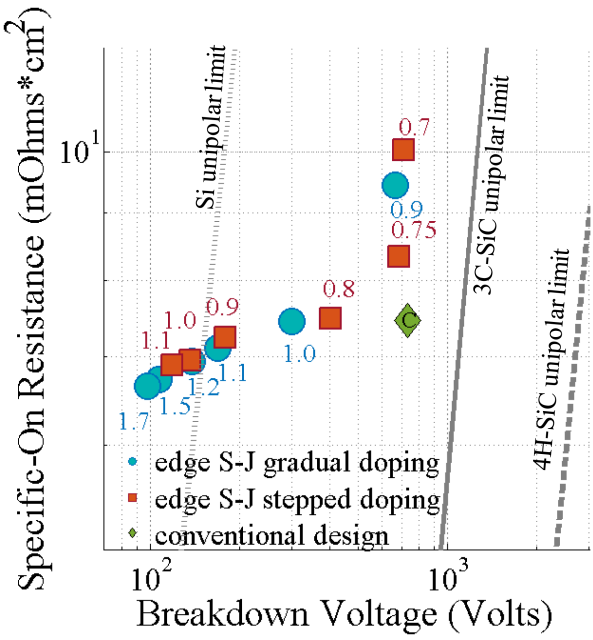

Fig. 7. The $R_{\rm DS,on}^{\rm sp}$ as a function of blocking voltage for the simulated devices. The points annotation corresponds to the percentage of the dose values listed in Table I considered for the particular design variant.

B. Specific On-Resistance

The ON-resistance is calculated for each simulated MOS-structure as the slope of the $I_D - V_D$ plot. The values of $V_D = 0.5$ V and $V_G = 10$ V have been selected to ensure the $R_{\rm DS,on}$ is calculated while all the simulated devices operate in the linear region. The specific ON-resistance ($R_{\rm DS,on}^{\rm sp}$), is then obtained, by multiplying the calculated ON-resistance with the active area of the devices. The $R_{\rm DS,on}^{\rm sp}$ against the blocking voltage plot, in Fig. 7, excludes the points that correspond to the design variants with a very high $R_{\rm DS,on}^{\rm sp}$ value due to insufficient

formation of the JFET. Therefore, from both Figs. 6 and 7, the acceptable charge imbalance window is redefined from -65% up to -45% for the S-J JFET design.

The simulated electrical performance in Fig. 7, in terms of $R^{\rm sp}_{\rm DS,on}$ and breakdown voltage, is compared with the 3C-SiC unipolar limit. This curve specifies the minimum specific ON-resistance of unipolar devices for the corresponding blocking voltage capabilities and constitutes a widely acceptable mean to discuss on the technological maturity of the power semiconductor. The unipolar limit for 3C-SiC is calculated with (7), as the trade-off relationship between the specific ON-resistance of a drift layer (forward operation mode) and the corresponding breakdown voltage (reverse operation mode) [32]. The expressions regarding the $V^{\rm 3C-SiC}_{\rm BR}$ and $E^{\rm 3C-SiC}_{\rm Cr}$ derived from the power formula for 3C-SiC [33] as a function of the doping concentration have been deployed in (7). The power formula for 3C-SiC and, hence, the derived expressions for the critical field and the breakdown voltage assume NPT structures for which all the drift is ideally depleted. For completeness, the unipolar limits for Si and 4H-SiC [34] are also plotted in Fig. 7.

$$R^{\rm sp}_{\rm DS,on} = \frac{4V^2_{\rm BR}}{\varepsilon_S \mu E^3_{\rm Cr}}. \tag{7}$$

In Fig. 7, the conventional or implanted-body design method for the 3C-SiC-on-Si MOSFET demonstrates a breakdown voltage very close to the one suggested by the 3C-SiC unipolar limit. However, it features a higher $R^{\rm sp}_{\rm DS,on}$ value. The same stands for the simulated ON-state performance of the proposed S-J JFET designs. The definition of the unipolar limit explains why we should expect a larger $R^{\rm sp}_{\rm DS,on}$ with MOSFETs. This definition assumes the specific ON-resistance of a drift layer. On the contrary, the total resistance of a vertical MOS-based device arises as the summation of the channel resistance ($R_{\rm ch}$), the JFET resistance ($R_{\rm JFET}$), the drift layer resistance ($R_{\rm drift}$), the buffer layer resistance ($R_{\rm buf}$), and the substrate resistance ($R_{\rm sub}$).

The developed model for the channel mobility shapes the $R_{\rm ch}$ contribution by taking into account the degradation of the electrons mobility at the $3{\rm C}-{\rm SiC}/{\rm SiO_2}$ interface. Further, both $R_{\rm buf}$ and $R_{\rm sub}$ have a reduced contribution to the device resistance as highly doped regions. The JFET effect is mainly responsible for the observed deviation of the specific on-resistance of the simulated MOSFETs from the 3C-SiC unipolar limit. The JFET effect induces a modified effective width for the current to flow, from the initial cell pitch value to a reduced one. This leads to a nonuniform current distribution within both the JFET and the drift regions, resulting in increased $R_{\rm JFET}$ and $R_{\rm drift}$ values, which also incorporate the effect from the formed depletion region, essentially increasing the total $R^{\rm sp}_{\rm DS,on}$.

C. Performance and Effectiveness of the S-J JFET Region

From Figs. 6 and 7, the "golden" design is identified to feature 75% of the dose values shown in Table I and with stepwise p-body doping profile. To demonstrate the effectiveness of the proposed "golden" design, the S-J region was removed by omitting the additional mask (process step b2 in Fig. 3). The electrical performance of the "non-S-J variant" was studied and compared with the "Golden design having S-J JFET." The simulated performance of the golden design summarized in Table III suggests that the proposed S-J JFET MOSFET based on 3C-SiC-on-Si is capable of exhibiting similar forward-blocking capabilities compared to a conventional method used to design MOSFETs

TABLE III
PROPERTIES AND PERFORMANCE OF THE SIMULATED GOLDEN 3C-SIC-ON-SI S-J JFET MOSFET DESIGN

		Golden design having S-J JFET	Golden design without S-J JFET	Theoretical/ Conventional design
Gate Oxide Thickness *(nm)*		60		
Fixed Charges *(cm^{-2})*		$2.5x10^{11}$		
p-body doping *(gradual / stepped)*		Stepped epitaxial	Stepped epitaxial	implanted
Charge Imbalance *(%)*		-59	-	-
Breakdown Voltage *(V)*	**T=300K**	688	387	734
	T=473K	790	530	810
Effective Channel Mobility (cm^2Vs^{-1}) at V_G=10V	**T=300K**	225	240	195
	T=473K	150	147	113
$R_{DS,on}(mOhms * cm^2)$	**T=300K**	8.3	5.9	7.5
	T=473K	16	11.7	16.6
Threshold Voltage *(V)*	**T=300K**	3.6	3.6	3.7
	T=473K	3.4	3.4	3.5

Considering $T = 300$ K, the simulated $R^{\rm sp}_{\rm DS,on}$ is slightly higher for the golden S-J JFET design compared to a theoretical implanted body design. This is attributed to the small number of *N* implantations used. With a larger number of implantations, the JFET profile can be further fine-tuned, leading to a MOSFET design with *in situ*-doped p-body having a resistance closer to the theoretical limit. At elevated temperature, the blocking capability of all variants examined increases. This is expected as the breakdown voltage in unipolar devices is determined by impact ionization-induced avalanche. Since the impact ionization rates decrease when the temperature increases, the blocking voltage increases [27]. At $T = 473$ K, the golden design achieves blocking voltage of 790 V. The predicted $R^{\rm sp}_{\rm DS,on}$ values follow the expected trend too. With increasing temperature, the $R^{\rm sp}_{\rm DS,on}$ increases too. Interestingly, the golden device exhibits slightly lower $R^{\rm sp}_{\rm DS,on}$ compared to the theoretical design at $T = 473$ K, whereas at $T = 300$ K, it was the opposite.

The golden design without S-J JFET can support only 387 V (at $T = 300$ K) compared to 688 V achieved when an S-J JFET is formed. The difference in performance is explained by studying the electric field distribution at 375 V (Fig. 8). As shown in

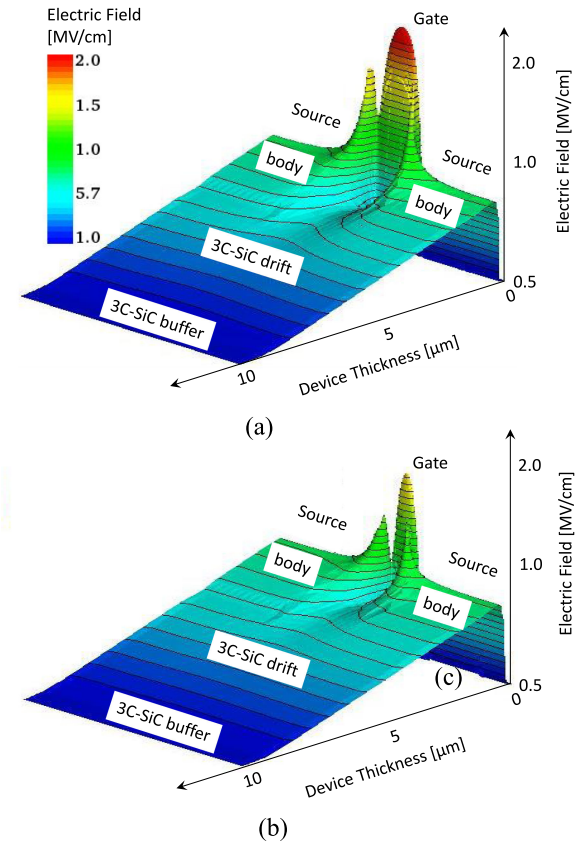

Fig. 8. Electric field plots at $T = 300$ K for (a) golden design without S-J JFET, and (b) golden design featuring extended p-body edges forming a local S-J region.

Fig. 8(a), in the absence of S-J region, the peak electric field at the corner between the p-body with the JFET region and at the bottom of the gate oxide reaches values in excess of $2\,\mathrm{MV cm^{-1}}$. The high electric field observed causes excessive impact ionization, which degrades the forward-blocking capability. In comparison, when an S-J region is formed by extending the p-body edge [Fig. 8(b)], the electric field is suppressed, leading to reduced impact ionization phenomenon and therefore higher breakdown voltage. This is true both at room temperature ($T = 300$ K) and high temperature, e.g., at $T = 470$ K.

D. Impact of Partial Overcompensation

The overcompensation of *in situ* doping with limited number of implantation steps can lead to the formation of thin p-type stripes of noncompensated regions remaining within the JFET. For as long as their thickness is smaller than the diffusion length (L_n) of electrons, these stripes add to the ON-resistance but do not completely block the electrons flow. In example, two edge S-J JFET MOSFET variants are considered featuring a thin and a thick p-type stripe correspondingly in the JFET. In Fig. 9, the equilibrium state of the conduction bands is illustrated after solving the initial Poisson equations with the TCAD sDevice tool and the boundaries of each stripe are indicated with dashed lines.

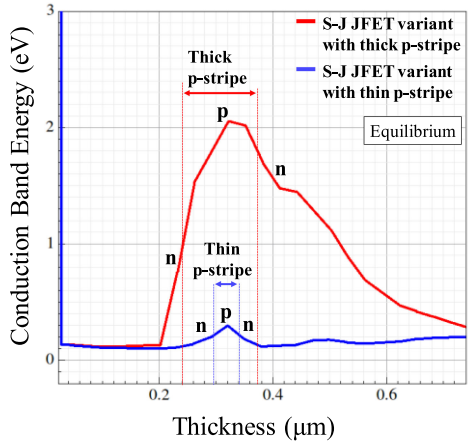

Fig. 9. Equilibrium state of a thick and a thin p-stripe in the overcompensated JFET corresponding to design variants with 70% and 90% of the dose values in Table I and a gradual p-body profile.

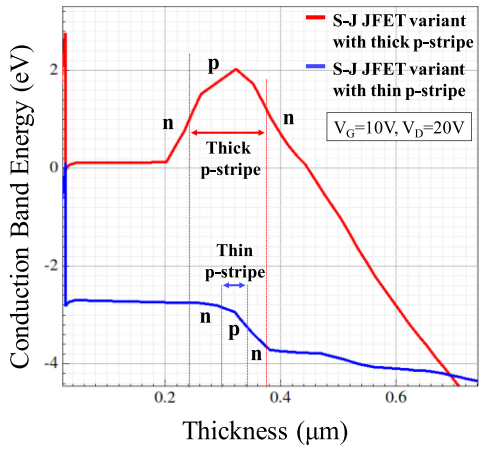

Fig. 10. Forward bias behavior of a thick and a thin p-stripe in the overcompensated JFET corresponding to design variants with 70% and 90% of the dose values in Table I and a gradual p-body profile.

In Fig. 10, the MOSFETs are biased with $V_G = 10$ V and $V_D = 20$ V, which are sufficient values to turn-ON the particular devices. Under these conditions ($V_G > V_{\mathrm{th}}$, $V_D > 0$), the top n-p diode of the thin p-stripe becomes forward-biased and minority electrons diffuse in the p-type region of the diode. The L_n of electrons allows them to reach at the boundary of the depletion region of the reversed bias bottom p-n diode. The injected electrons that are not recombined within the hostile p-type environment are accelerated to the n-type region because of the enhanced electric field at the space charge region of the p-n diode. In consequence, in the S-J JFET design variant with the thin p-stripe, electrons are free to diffuse from left to the right direction. On the other hand, the n-p diode of the thick p-stripe, with the initially fully deployed built-in potential, still obstructs the free electrons' flow with a potential barrier, resulting in a largely increased $R^{\mathrm{sp}}_{\mathrm{DS,on}}$.

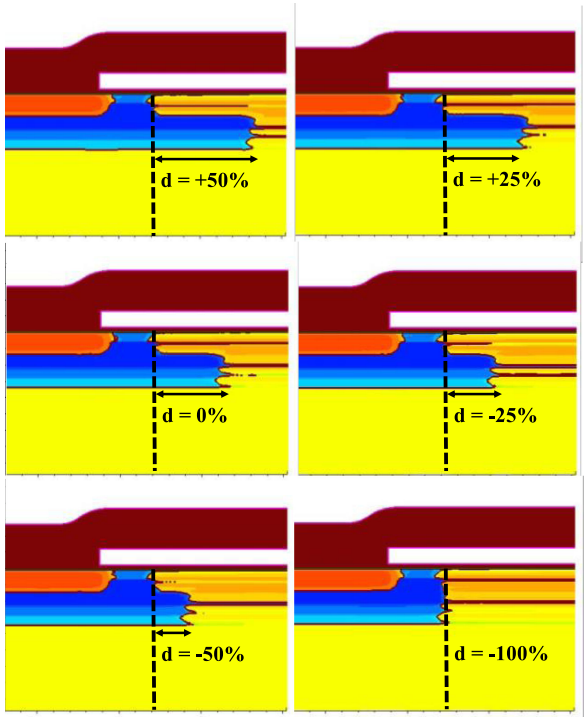

Fig. 11. A first performance sensitivity analysis considered varying the S-J edge length by delta (d) in reference to the golden design.

E. Sensitivity to Geometric Variations

The performance and the characteristics of the MOSFET devices following the proposed process flow could become sensitive to the device dimensions. In this subsection, the performance sensitivity is investigated by the means of the S-J edge length (ledge) and the channel length.

A first sensitivity analysis was carried out considering the S-J ledge as a design variable, whilst the channel length is considered constant (Fig. 11). Each simulated structure features a ledge which differs by delta (d) with regards to the golden design, which is used as the reference design. The values of d for this first analysis are assumed -50%, 25%, $+25\%$, and $+50\%$. In addition, the case of $d = -100\%$ is also considered, which corresponds to the golden design without the S-J part. The simulated structures for this first sensitivity analysis are illustrated in Fig. 11, where the golden design corresponds to a d value of 0%.

The results are illustrated in Fig. 12 and Table IV. For a variation of ledge by $+25\%$, the $R^{\text{sp}}_{\text{DS,on}}$ increases by $\sim$18% at $T = 300$ K and by $\sim$16% at $T = 473$ K whereas the breakdown voltage increases by $\sim$5% at $T = 300$ K and by $\sim$2% at $T = 473$ K. For a variation of ledge delta by -25%, the impact is somewhat less; the $R^{\text{sp}}_{\text{DS,on}}$ drops by $\sim$11% at $T = 300$K and by $\sim$9% at $T = 473$ K whereas the breakdown voltage drops by $\sim$13% at $T = 300$ K and by $\sim$10% at $T = 473$ K. It is therefore safe to conclude that the impact of ledge variation is small on the breakdown voltage (smaller than $\sim$13% for 25% variation) whereas the impact on $R^{\text{sp}}_{\text{DS,on}}$ is at least better than

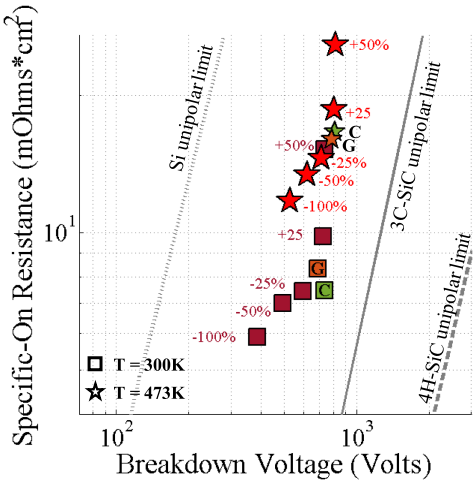

Fig. 12. The $R^{\text{sp}}_{\text{DS,on}}$ as a function of blocking voltage for simulated structures with the S-J edge length changing by delta (d), with regards to the golden design, and for various temperatures.

TABLE IV
PERFORMANCE SENSITIVITY AS A FUNCTION OF S-J EDGE LENGTH

Ledge delta (d) compared to Golden Design (%)	**Charge Imbalance** *(%)*	**Breakdown Voltage** *(V)*		$R_{DS,on}$ $(mOhms * cm^2)$	
		300K	**473K**	**300K**	**473K**
-100% (Golden without S-J part)	-	387	530	5.9	11.7
-50%	-216	493	624	7	13.4
-25%	-111	598	713	7.4	14.5
0% (Golden Design)	-59	688	790	8.3	16
+25%	-10	723	805	9.8	18.6
+50%	13	737	817	15.2	25.7

TABLE V
PERFORMANCE SENSITIVITY AS A FUNCTION OF CHANNEL LENGTH

Channel length delta compared to Golden Design (%)	**Charge Imbalance** *(%)*	**Breakdown Voltage** *(V)*		$R_{DS,on}$ $(mOhms * cm^2)$	
		300K	**473K**	**300K**	**473K**
-50%	-29	662	770	8.09	15.85
-25%	-45	658	764	8.31	15.93
0% (Golden Design)	-59	688	790	8.32	16
+25%	-80	691	780	8.55	16.3
+50%	-92	695	785	8.66	16.96

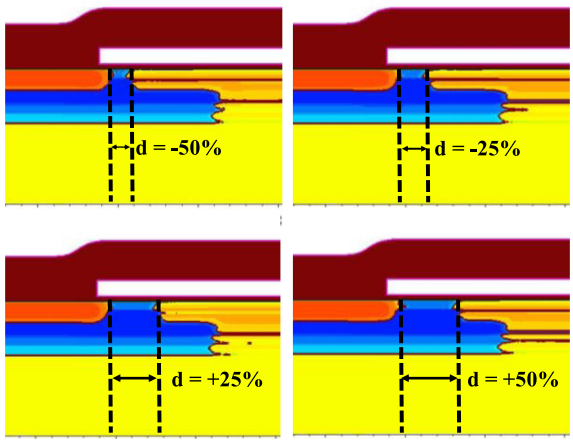

Fig. 13. The $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ as a function of blocking voltage for simulated structures with the S-J edge length changing by delta (d), with regards to the golden design, and for various temperatures.

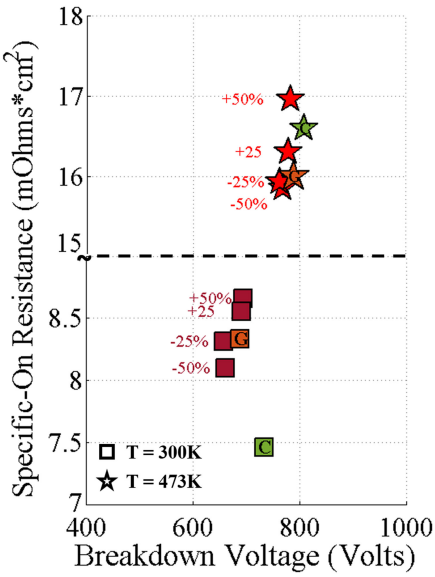

Fig. 14. The $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ as a function of blocking voltage for simulated structures with the channel length changing by delta (d), with regards to the golden design, and for various temperatures.

proportional to the variation exhibited (smaller than $\sim$18% for 25% variation).

A second sensitivity analysis was carried out considering the channel length as variable, whilst the S-J ledge considered constant (Fig. 13). The results are shown in Fig. 14 and Table V. The impact of channel length on $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ and the breakdown voltage is small; for 25% variation, the impact on $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ is $\sim$2% or less and the impact on breakdown voltage is $\sim$4% or less. This performance is significantly better than what is expected from a conventional design (no edge extension of body). This is because a variation in the channel length with ledge kept constant does not change the minimum distance between the two p-body regions of the MOSFET. The latter is not the case in conventionally designed devices. It is hence safe to conclude that the extended body regions help to decouple the channel length from the important performance parameters of $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ and breakdown voltage.

VI. Conclusion

In this article, a novel S-J JFET process for viable vertical 3C-SiC-on-Si n-MOSFETs is proposed, disrupting current material related limitations. Instead of utilizing ion implantation to form the p-body region, a thin layer of p-type conductivity can be grown by homoepitaxy. Thereafter, a JFET region with localized S-J region can be created via N implants which overcompensate the p-type layer in a nonuniform manner. To assess the proposed MOSFET fabrication method and design it was important to develop and validate a channel mobility degradation model for 3C-SiC MOS structures which takes into consideration the weighted degradation contribution due to doping level ($\mu^{\mathrm{3C-SiC}}_{\mathrm{dop}}$), electric field ($\mu^{\mathrm{3C-SiC}}_{E//}$), scattering phenomena and temperature. By implementing the model in TCAD, a relatively wide safe charge imbalance window, from -65% up to -45%, was identified which can accommodate for uncertainties in the final net doping concentration value. Further, the proposed design was shown to have relatively small sensitivity to variations in channel length and the length of the S-J region. The golden design, following the S-J JFET process, not only enables the 3C-SiC-on-Si MOSFET technology, but also has the potential to offer excellent ON-state, high channel mobility values, and forward-blocking capabilities for a wide range of temperatures (300 K $\leq T \leq$ 473 K), similar to the theoretical design method for MOSFETs. The proposed process could be applicable on any WBG material technology which experiences limited p-type implants activation.

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