Short-Circuit Performance Investigation of 10kV+ Rated SiC n-IGBT

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***Abstract*—This paper presents a comprehensive short-circuit robustness investigation of 4H- Silicon Carbide (SiC) n-type Insulated Gate Bipolar Transistors (nIGBTs) for Medium-Voltage and High-Voltage applications. Numerical electrothermal TCAD simulations evaluate the IGBT short-circuit behaviour under various conditions and device parameters variation. The internal device current density and temperature distribution show that the parasitic thyristor latch-up and the thermally-assisted leakage current generation can be the failure mechanism of SiC nIGBT when the device temperature in the p-well/n-emitter interface region is about 1500K.**

Keywords— SiC IGBT, short-circuit capability, parasitic thyristor latch-up, electrothermal simulation

I. INTRODUCTION

Silicon Carbide (SiC) IGBTs can improve the efficiency and expand the operational limits of power semiconductor devices in higher voltage, current, frequency or power density and offer more margins in power converters design due to the superior characteristics of the SiC material. However, as the operating voltage and currents increase, so does the demand for a wider safe operating area to improve the reliability and power handling capability[1].

Most of the research effort has been put into reducing the power losses of the SiC-IGBT by optimising the trade-off between on-state and switching losses [2]-[3]. However, there is a fundamental trade-off between the Safe Operating Area (SOA) and power losses. Recent studies have shown that IGBT accounts for nearly 34% of failures in converter systems [4]-[5]. Short circuit destruction is one of the most common failures of IGBTs operating in motor drive or power conversion applications. Although this failure is usually caused by external factors, such as false gate triggering or load short-circuiting, it can permanently destroy the device because of the simultaneous occurrence of high voltage and high current for an extended time, leading to extremely high-power losses and an increase in lattice temperature. As a result, the IGBT can fail thermally due to parasitic thyristor latch-up, thermal runaway, or contact failure when the surface IGBT temperature increases above the eutectic temperature between metal and semiconductor [6].

Therefore, the IGBT must be capable of handling this high power until the protection circuits are activated and prevent the IGBT from permanent destruction. It is also required to turn the IGBT off safely after detecting the short circuit without destruction. Typically, short-circuit withstand time (SCWT) of 10μs is enough for the protection circuits to safely operate and turn off the IGBT.

For SiC IGBTs, only a few studies have been focused on short-circuit capability. In [7], a novel IGBT structure with a lateral JFET region is proposed to limit the saturation current linked with the short-circuit capability. However, this study has not presented the device's internal current densities or the hot-spot's location. More recently, the short circuit behaviour of a SiC IGBT was demonstrated in [8] with simulation and experimental results. However, the focus was to turn off the IGBT as fast as possible, and as a result, the entire short-circuit behaviour was not presented.

Therefore, it is essential to understand the destruction mechanisms of the short-circuit failure modes and the impact of various device and circuit parameters on the short-circuit ruggedness of the device. This paper presents a wide range of electrothermal TCAD simulations that can be used as input to support the design automation of high voltage SiC IGBTs.

The rest of this article is organised as follows. Section II presents the TCAD modelling approach and the simulation test setup. In Section III is presented the equivalent circuit representation of the IGBT using discrete components and their temperature dependance is discussed. The short-circuit failure modes of the IGBT are analysed and described in Section IV, and a parameter sensitivity analysis is presented in Section V. Finally, Section VI concludes the paper.

II. DEVICE STRUCTURE, MODELING AND SIMULATION

Sentaurus TCAD simulation platform was used to implement the 4H-SiC IGBT structure shown in Fig 1(a). The doping concentration of the p+ injector, n buffer layer and n- drift layer are 1×10^{19}, 5×10^{17} and 3×10^{14} cm^{-3}, respectively. The thicknesses are 4, 3 and 100 μm, respectively. The doping profile of the p well is retrograde, featuring a lower surface doping of $5x10^{17}$ and a maximum doping concentration of 1.8×10^{18} cm^{-3} at a depth of 0.5 μm, which gradually reduces

to 3×10^{14} cm^{-3} at a depth of 2 µm as shown in Fig. 1(c). The gate oxide thickness is 86nm giving an approximate gate threshold voltage of 5.5V at room temperature (RT). The above values achieve a breakdown voltage of about 13.5kV at RT, thus allowing to class the device at 10kV (Fig. 1(d)).

The fabrication procedure was simulated using Sentaurus TCAD process simulation, and the short-circuit performance was evaluated using the topology shown in Fig. 1(b). The simulation uses previously calibrated models for critical semiconductor physics [9]–[11], including incomplete ionisation, impact ionisation, Shockley-Read-Hall (SRH) and Auger recombination, doping and temperature dependence and anisotropy of mobility, fixed charge and interface traps at the oxide – semiconductor interface. Additionally, non-isothermal equations are incorporated to account for the self-heating effects within the semiconductor.

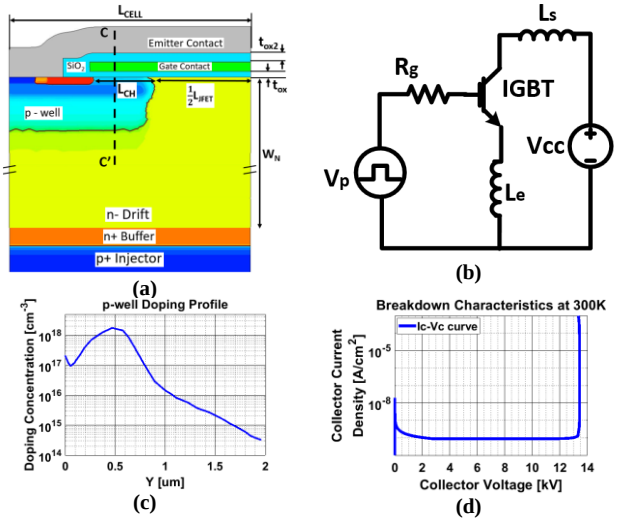

Fig. 1. (a) n-channel IGBT half-cell; (b) short-circuit schematic; (c) p-well doping concentration profile; (d) breakdown waveform.

III. IGBT Internal Current Distribution and Temperature Dependance

The IGBT equivalent circuit shown in Fig. 2 is used to study the internal current distribution and to understand the device behaviour. The IGBT structure is similar to a MOSFET, except having a highly doped p-type injection region. As a result, the IGBT can be represented by a series connection of a PiN diode with an n-type MOSFET. The diode component effectively reduces the resistance of the drift region by injecting plasma. Additionally, the p+ injector n+ buffer/n- Drift and p well are equivalent to a wide base PNP and an NPN bipolar junction transistor coupled together to form a four-layer thyristor structure.

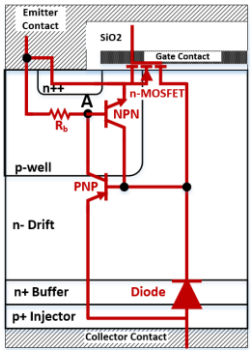

Fig. 2. Illustration of the parasitic components within the IGBT device structure.

During the normal operation, the parasitic NPN transistor is not active and does not contribute to the conductivity of the IGBT. The electron current flowing through the channel (I_n) acts as a base current for the wide base PNP transistor and therefore a hole current (I_p) flowing across the p-well region according to Eq. 1 where β_{PNP} is the common emitter and α_{PNP} the common base current gains. The total collector and emitter current are the sum of the electron and hole current components and are given by Eq. 2.

$$I_p = \beta_{PNP} = \frac{\alpha_{PNP}}{1 - a_{PNP}} I_n \quad (1)$$

$$I_E = I_C = I_n + I_p = \frac{I_n}{1 - a_{PNP}} \quad (2)$$

Under short circuit conditions the current is limited by the MOS channel saturation current given by Eq. 3 and as a result the total collector saturation current is given by Eq. 4.

$$I_n = \frac{\mu_{ns} C_{ox} Z}{2W_{CH}} (V_{GE} - V_{Th})^2 \quad (3)$$

$$I_c = \frac{\mu_{ns} C_{ox} Z}{2W_{CH}(1 - a_{PNP})} (V_{GE} - V_{Th})^2 \quad (4)$$

The C_{ox} in the above equations is the gate oxide capacitance, V_{th} is the gate threshold voltage, μ_{ns} the channel mobility, W_{CH} the channel length and Z the width of the device orthogonal to the cross section.

The hole current flowing though the p-well generates a voltage drop across the parasitic resistance R_b shown in Fig. 2. This parasitic resistance can be approximated by Eq. 5, where N_{Pwell} and D_p are the doping concentration and thickness of the high doped region of the retrograde p-well, W_{n++} is the length of the n_{++} emitter region, and μ_p the hole mobility. When this voltage drop increases above the built-in potential (Eq. 6) of the base to emitter junction of the parasitic NPN transistor, this transistor is activated and triggers a positive feedback mechanism and the short circuit current rises uncontrollably. Figure 3 shows the temperature dependence of the current-voltage characteristics of a PiN diode in the range between 300K and 1200K. It can be seen that as the temperature increases, so does the intrinsic carrier concentration and the built-in potential of the diode reduces.

$$R_b = \frac{W_{n++}}{q\mu_p N_{Pwell} D_p Z} \quad (5)$$

$$\varphi_{bi} = \frac{kT}{q} \ln\left(\frac{N_{Pwell} N_{n++}}{n_i^2}\right) \quad (6)$$

The k in Eq. 6 is the Boltzman constant, T is the temperature in Kelvin, N_{n++} is the n++ region doping concentration and n_i is the intrinsic carrier concentration.

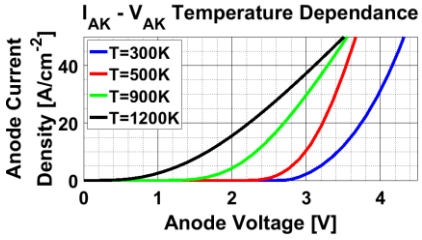

Fig. 3. Temperature dependence of the built-in potential in a PiN diode.

It is worth mentioning that apart from the built-in potential (Eq. 6), many of the parameters used in the previous equations are temperature dependent. The threshold voltage of the MOS structure is a complex function of the doping density, contact-semiconductor work function, fixed oxide charge and

interface charge, and as a result the threshold voltage is strongly dependent on the temperature as can be seen in Fig. 4.

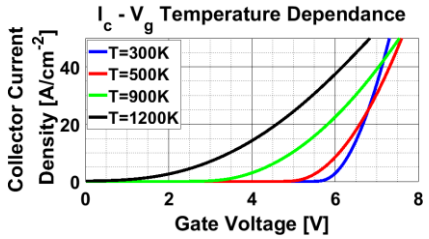

Fig. 4. Temperature dependence of the gate threshold voltage on a SiC IGBT.

Additionally, the current gain of the IGBT increases with temperature increase due to the higher dopant activation at elevated temperatures. Finally, the electron and hole mobilities and other process dependent parameters are strongly dependent on temperature and play a critical role in the short circuit behavior of the IGBT. A more detailed description of the temperature dependence of the above mentioned parameters can be found in [12].

As a result, non-isothermal equations are used to account for self-heating effects in all simulations presented below to describe the short circuit mechanisms and the impact of various design parameters.

IV. IGBT Short-Circuit Mechanisms

The general short circuit characteristics are studied using a Sectaurus TCAD mixed-mode simulation. The DC bus voltage (V_{cc}) is set to 5kV, about 40% of the breakdown voltage. The gate voltage pulse (V_p) has a value of 15V and the gate resistance of 7.5 Ohm. The stray inductance (L_s) and the parasitic emitter inductance (L_e) are 100nH and 10nH, respectively. The thermal boundary conditions where set by using a thermal electrode in the collector side with initial temperature 373K (100ºC) and surface thermal resistance 0.034 Kcm^2/W which is similar to what was used in studies for SiC MOSFETs [13][14]. These are the parameters for the reference case but will be varied in the parameter sensitivity analysis in Section IV.

Although the reason for the IGBT destruction in a short circuit event is the high power dissipation which increases the device temperature, the processes leading to the breakdown may vary depending on the failure mode as described below.

A. *Parasitic thyristor Latching during steady-state*

Figure 5 shows the emitter current, gate and collector voltages and the maximum temperature within the device. An analysis of the equivalent circuit representation of the IGBT, shown in Fig. 2 with the internal temperature, electron, hole and total current density inside the device at different times of the short-circuit event (Fig. 6) can help to understand the failure mechanisms.

The short circuit current waveform can be divided into three phases as follows.

Phase I (3-6μs): At the beginning of the short-circuit event, the current increases quickly due to the small inductance, and the device enters the saturation region. However, the current keeps increasing because of the positive temperature coefficient of the MOS channel mobility up to about 600K due to the release of trapped electrons at higher temperatures, as has been reported in [15][16]. As a result, the electron current injected into the drift region keeps increasing. Since this electron current constitutes the base current of the wide-base PNP transistor, the holes injected from the p+ injector reaching the p well increase. This results in an increase of the hole current component through the p-well to the emitter contact.

Phase II(6-23μs): As the IGBT operates at high voltage and current conditions, the device temperature increases above 600K, and the current waveform takes a negative slope due to several reasons. Firstly, as the temperature further increases, all trapped electrons in the oxide/semiconductor interface have been released and the coulomb scattering is increased [16]. Additionally, the carrier mobility in the MOS and drift region is reduced at extremely high temperatures. Furthermore, as presented in [17], the carrier lifetime exhibits a negative temperature coefficient at temperatures higher than 673K due to the activation of a higher number of recombination centres.

Phase III (23μs - failure): At this phase, the maximum device temperature exceeds 1300K and the thermal phenomena within the device trigger a positive feedback mechanism of current increase which eventually leads to its failure. More specifically:

- The p-well resistance, R_b in Fig. 2, increases and hence a higher voltage drop is induced in point A, leading to a higher base current of the NPN.
- The gate threshold voltage of the MOSFET reduces (Fig. 4); hence more electrons are injected into the drift region, serving as the base current of the PNP transistor.
- The built-in potential of all the PN junctions decreases with temperature increase (Fig. 3). Hence:
  - the NPN transistor opens at a lower base voltage.
  - the PiN diode injects more holes which serve as base current of NPN transistor.
  - PNP current gain increases; hence the PNP transistor injects more holes which serve as base current of NPN transistor.
- The carrier generation also increases with temperature contributing to the conduction of the device. According to [18], a temperature of more than 1400C is required to generate a carrier concentration of about $3.5x10^{15}$ cm^{-3}.

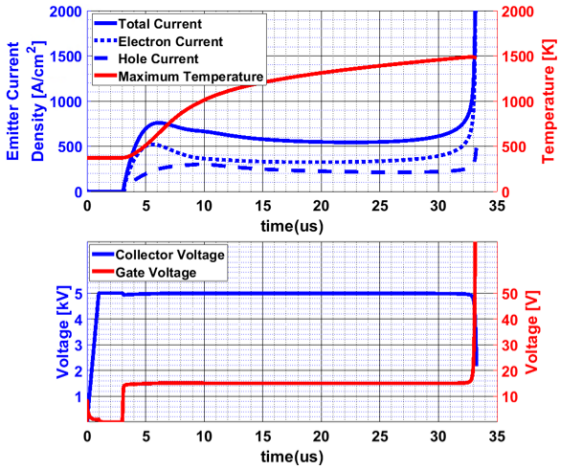

Fig. 5. Short circuit current and maximum device temperature (top); collector and gate voltage (bottom) during the short circuit failure.

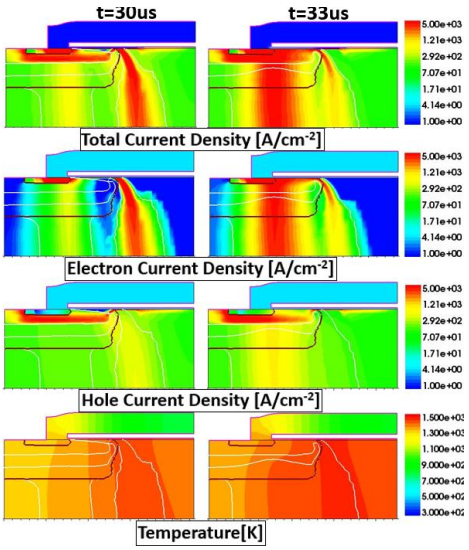

Fig. 6. Internal device current densities and temperature distribution before and after short-circuit failure.

B. *Leakage current failure during blocking state*

Apart from the above-described failure mechanism, the IGBT can fail several microseconds after the turn-off. Similar behaviour has also been observed in silicon IGBTs [19] and SiC MOSFETs [20]. Figure 7(a) shows the IGBT is turned off 3µs before its destruction (t=30µs). Even though the collector current falls after the gate voltage reduces below the threshold voltage, the leakage current is high (18A/cm^2) due to the high temperature of the device. The increased carrier generation and the threshold voltage reduction at higher temperatures can explain this high leakage current, as described earlier.

Furthermore, during the current conduction mode, the hot spot location is close to the gate oxide in the JFET region due to the higher portion of the electron current through the channel. However, during the blocking state, the heat starts spreading towards the thyristor part and the collector side of the IGBT, as shown in Fig. 7(b). As a result, more carriers are generated in the p-well region and the built-in potential of the base to emitter junction of the NPN transistor reduces. Eventually, the NPN transistor is activated, current start rising uncontrollably, the parasitic thyristor latches and the device fails.

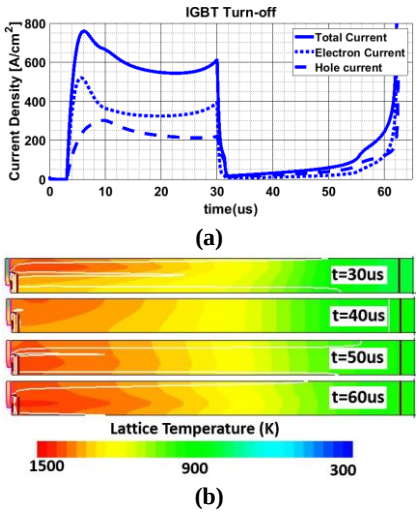

Fig. 7. (a) Emitter electron, hole and total current density before and after turn-off at 30µs; (b) Lattice temperature at various instants after IGBT turn-off.

V. Parameter Sensitivity Analysis

Many circuit and device-related parameters impact the short-circuit robustness of the IGBT. The impact of each of them are presented and discussed below:

A. *DC bus voltage*

Figure 8 shows the impact of the DC bus voltage variation. The SCWT varies from 5µs at 8kV to almost 100µs at 2kV. The apparent reason is that the power dissipation is higher for higher DC bus voltage, leading to a faster increase in the lattice temperature. Additionally, it can be seen that the maximum temperature at the time of failure is lower as the DC bus voltage increases. This can be explained by the fact that the current gain of the internal PNP transistor increases as the collector voltage increases because of the higher depletion width of the drift region. As a result, the hole current density through the p-well is higher, and the parasitic thyristor latches at a lower temperature.

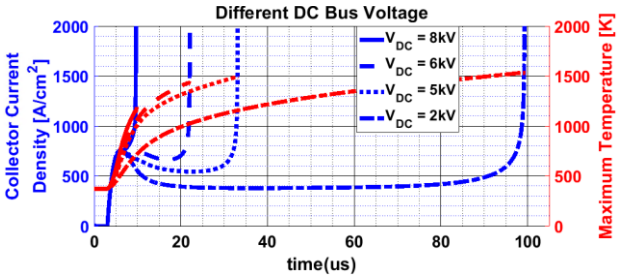

Fig. 8. IGBT short-circuit behaviour with different DC bus voltages.

Additionally, for lower DC bus voltages, or higher SCWT, the temperature spreading in the emitter side of the semiconductor is different as shown in Fig. 9. The higher temperature in the intermetal oxide and the emitter contact for the DC bus voltage of 2kV can lead to fracture of the oxide (due to different thermal expansion coefficients of the materials) or melting of the aluminium contact. As a result a different failure mechanism might be observed similarly to what presented for SiC MOSFET in [14]. However, to study this failure mechanism, a mechanical stress analysis is required, and the thermal resistance and capacitance of the emitter contact should be considered which are beyond the scope of this paper.

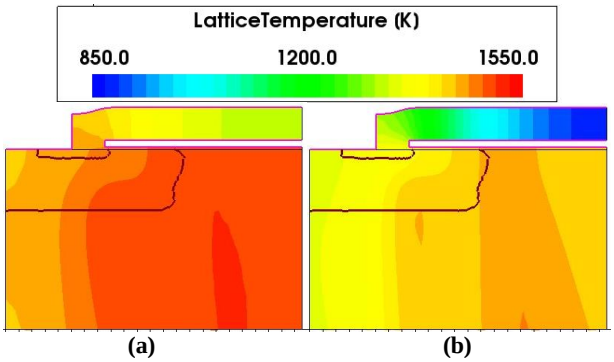

Fig. 9. Temperature distribution in the emitter side of the IGBT during the short circuit failure under (a) V_{DC} = 2kV at 99us and (b) V_{DC} = 5kV at 33us.

B. *Gate Voltage*

The gate voltage strongly affects the short-circuit ruggedness of the IGBT as it controls the electron current density through the channel. Therefore, by reducing the gate voltage of an IGBT, the magnitude of the fault current is reduced and the SCWT is extended, as shown in Fig. 10.

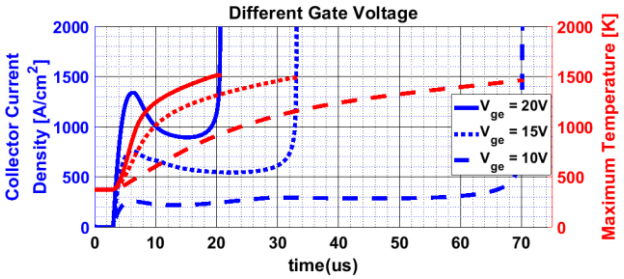

Fig. 10. IGBT short-circuit behaviour with different gate voltages.

C. *Gate resistance, stray inductance and lattice temperature*

Figure 11 shows the impact of the gate resistance, stray inductance, and lattice temperature at the beginning of the short-circuit phenomenon. The two first parameters only affect the transient phenomena and do not contribute significantly to the temperature rise of the IGBT. Additionally, even when the initial lattice temperature before the short-circuit increase from 373K to 900K, the SCWT is not significantly reduced due to the carrier mobility reduction at higher temperatures. Finally, the heat transfer properties of the backside packaging seem to have minor effects on the SCWT due to the fast evolution of the short-circuit event.

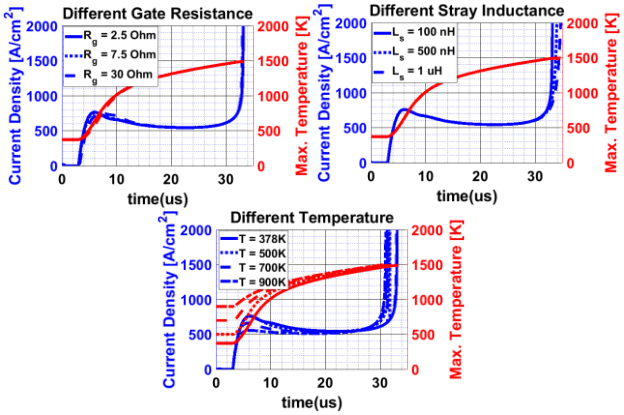

Fig. 11. The influence of the gate resistance, stray inductance and lattice temperature on the short circuit robustness of the IGBT.

D. *Channel and JFET width*

Figure 12 shows the impact of the channel and JFET width on the SCWT. To keep the cell pitch constant for all the scenarios, the sum of the JFET and channel width is kept at 6µm. Smaller channel width increases the channel saturation current, and increased JFET width reduces the JFET region resistance. As a result, IGBTs with small channel length are less robust during the short circuit events.

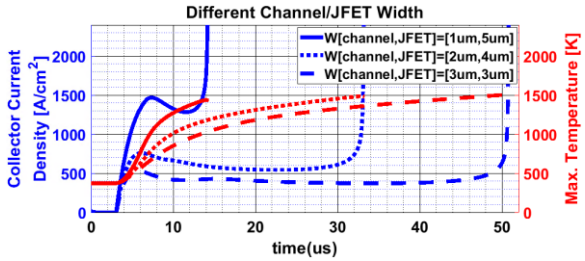

Fig. 12. IGBT short-circuit behaviour with different channel and JFET width.

E. *Buffer layer doping*

The Buffer layer doping controls the plasma injection into the drift region and the current gain of the PNP transistor. Therefore, the short circuit robustness can be also controlled by the buffer layer doping density. As a result, the high gain IGBTs come with the cost of lower SCWT, as shown in Fig. 13.

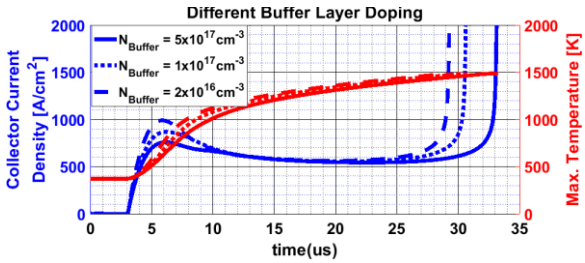

Fig. 13. IGBT short-circuit behaviour with different buffer layer doping density.

F. *P-well bottom doping*

The highly doped region of the p-well improves the latch-up immunity of the IGBT by reducing the equivalent resistance (R_b in Fig. 2). Consequently, the voltage drop across this resistance is lower, resulting in the thyristor latching-up at a higher temperature, as shown in Fig. 14.

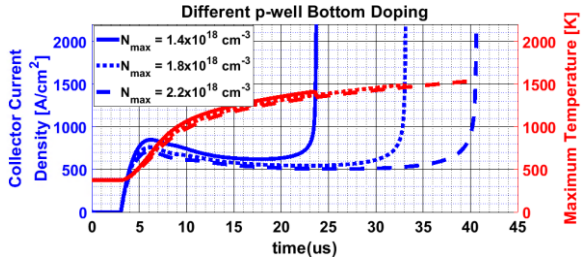

Fig. 14. IGBT short-circuit behaviour with different bottom p-well doping density

G. *N++ emitter region width*

Variation in width of the n++ emitter region has the same result in the p-well resistance. Therefore, the equivalent p-well resistance is also reduced by reducing its width and the SCWT increases (Fig. 15).

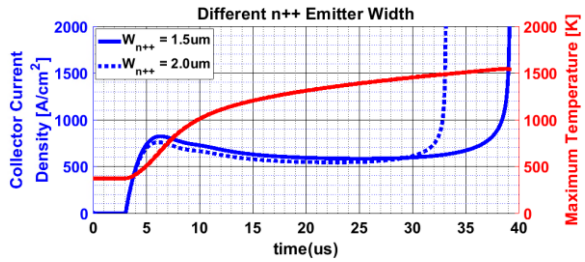

Fig. 15. IGBT short-circuit behaviour with different n++ emitter region width.

H. *Different turn-off time*

Moreover, it is worth pointing out the necessity of detecting and clearing the short circuit event as fast as possible to avoid high temperature and high leakage current generation during the blocking state. As shown in Fig. 16, even if the IGBT is turned off 6µs before its thermal breakdown, the positive feedback mechanism of leakage current increase eventually leads to failure after hundreds of microseconds.

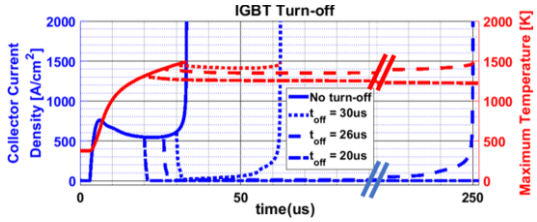

Fig. 16. IGBT short-circuit behaviour after turn-off at different times.

Finally, it is worth noting that because the failure can occur several hundred of microseconds after the turn-off, the system cannot be longer considered adiabatic, and the collector side thermal resistance plays a critical role in the cooling of the device. Additionally, because the maximum temperature is in the vicinity of the emitter side, the thermal properties of the emitter contact should also be considered to obtain accurate results [13]. As a result, the emitter metallisation and aluminum bond wire thermal properties should also be taken into account in future work.

VI. Conclusions

In this paper, the short circuit performance of a 10kV+ SiC IGBT has been investigated by electrothermal simulations. The internal current density and temperature distributions revealed that the parasitic thyristor latch-up is the failure mechanism of the IGBT when the maximum temperature in the p-well region is about 1500K. As a result, the importance of detecting and clearing a short-circuit event in the initial stages of the phenomenon is highlighted. Additionally, the influence of several circuit and device level parameters on the short circuit robustness were studied. It can be concluded that various device parameters can be adjusted accordingly to achieve the desired short-circuit withstand time for specific applications and system requirements.

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