On the Static Performance of Commercial GaN-on-Si Devices at Elevated Temperatures

Perkins S.[a], Arvanitopoulos A.[a], Gyftakis K N.[a], Lophitis N[a].
[a] Faculty of Engineering, Environment and Computing
[a] Coventry University
Coventry, UK
Perkin19@uni.coventry.ac.uk

Abstract—**This work provides an experimentally driven comparison between commercialized Gallium Nitride on Silicon (GaN-on-Si) and Silicon (Si) Super Junction (S-J) power devices at elevated temperatures. Elevated temperature experiments were performed to analyze the static performance of the Panasonic PGA26C09DV Enhancement (E-mode) p-GaN layer Gate Injected Transistor (GIT), the Transphorm TPH3206LD, TPH3206PD cascode GaN High Electron Mobility Transistors (HEMTs) and the Infineon SPA15N60C3 Silicon S-J. The Device Under Tests (DUTs) were characterized in a thermal chamber using the B1505A Power Device Analyzer. The elevated temperature measurements were taken; analyzed and compared. The performance of the GaN-on-Si indicated a strong robustness in thermally challenging environments and demonstrated superior performances at higher temperatures in comparison to traditional Si S-J technology.**

***Keywords— B1505A, cascode GaN, E-mode, GaN HEMT, high temperature, power devices, static performance*.**

I. Introduction

In thermally challenging environments Gallium Nitride on Silicon (GaN-on-Si) based power devices theoretically offer considerable advantages to traditional Silicon technology due to GaN's innate material properties [1]–[4]. It is considered for existing Silicon power Field Effect Transistor (FETs) the average junction temperature (T_j) is within the region of 100–110 ºC [5]. For applications like Pulse Width Modulation (PWM) converters this equates to significant financial and design investments into the cooling system. In contrast, GaN based devices have the capability to operate at 200 ºC [1]. Being capable of operating at this high T_j has a significant impact for achieving greater power density levels in air cooled PWM converters [6]. Although, it should be stated that the effective integration of GaN based High Electron Mobility Transistors (HEMTs) in existing converters and applications will require several challenges to be overcome by the system engineer [7].

Manufactures have proposed several types of commercial GaN-on-Si power devices; arguably the two most successful devices are the p-GaN GaN-on-Si Gate Injected Transistor (GIT) and the cascode GaN-on-Si HEMT. These devices are inherently different in the way the device approaches normally-off operation. The Panasonic p-GaN GaN-on-Si GIT contains a p-doped GaN region below the gate to shift the potential across the channel underneath the gate. In contrast, the Transphorm cascode GaN-on-Si HEMT is a composite device containing a Low Voltage (LV), normally off, Silicon Metal Oxide Semiconductor FET (MOSFET) and a normally on GaN-on-Si HEMT device and therefore, not inherently an Enhancement mode (E-mode) power device. The cross-sectional views, band diagrams and topology for these devices is documented in [8]. The Panasonic PGA26C09DV E-mode p-GaN layer GIT and Transphorm TPH3206PD and TPH3206LD devices are GaN-on-Si power devices rated at 600 V. This effectively places them into competition with traditional Si technology. The comparable performance of these devices is therefore, extremely important for a system engineer's product choice and will impact the size, efficiency and performance of the overall system.

The development of GaN-on-Si technology has seen the introduction of ultra-low inductance packages for high frequency applications [9]. The Transphorm TPH3206LD is one such example, enclosed in an 8x8 PQFN package. In contrast, the remaining Device Under Tests (DUTs) discussed in this work are enclosed in the TO-220 package. This presents an additional consideration for system engineers in terms package trade-offs. Subsequently, in this work we analyze the performance of the Infineon SPA15N60C3 Silicon Super-Junction (S-J), the Panasonic PGA26C09DV E-mode p-GaN layer GIT, the Transphorm TPH3206PD and TPH3206LD cascode GaN-on-Si HEMT devices [10]–[13]. The DUTs are subjected to reverse I-V (I_{ds}-V_{ds}), Transfer characteristics (I_{ds}-V_{gs}), on-state resistance (R_{ON}) and breakdown voltage (BVDSS) measurements, to determine the high-temperature static performance of these devices.

TABLE 1. DEVICES UNDER TEST

Manufacturer	Type of DUT	DUT Model	Rated class	No. of Devices
Transphorm	*Cascode*	*TPH3206LD*	*600V/17A*	*10*
Transphorm	*Cascode*	*TPH3206PD*	*600V/17A*	*10*
Panasonic	*P-GaN GIT*	*PGA26C09DV*	*600V/15A*	*2*
Infineon	*S-J*	*SPA15N60C3*	*650V/15A*	*3*

The remaining sections of this paper are presented as follows; in section II the experimental setup and methodology is stated. In section III the experimental results and discussion is presented and finally in section IV this paper's conclusion is presented.

Authorized licensed use limited to: Cyprus University of Technology. Downloaded on August 05,2024 at 09:50:15 UTC from IEEE Xplore. Restrictions apply.

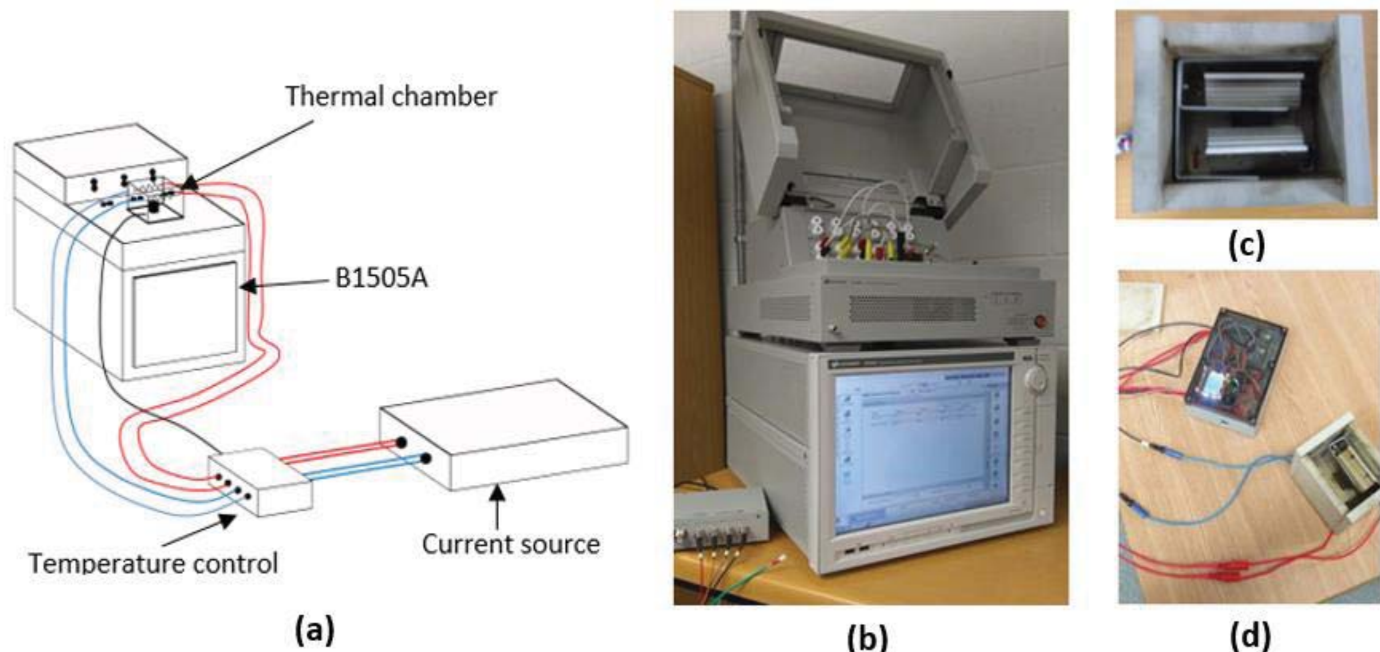

Fig. 1: (a) Graphical representation of the overall experimental setup, (b) The B1505A Power Device Analyzer, (c) Thermal chamber using resistive heating, (d) The thermal chamber connected to the temperature controller.

II. Experimental Setup and Methodology

A. Experimental Setup

A high-temperature polyetheretherketone (PEEK) chamber was fabricated to house the DUTs during elevated temperature experiments. The thermal chamber is illustrated in Fig. 1 (c) and (d). The thermal chamber housed two internal power resistors connected in parallel, illustrated in Fig. 1 (c). The two resistors dissipate a total power of 162 W. In addition, a metallic Aluminum conduction plate and lid was inserted into the thermal chamber to encourage uniform temperature through thermal conduction. Temperatures were elevated by supplying approximately 9 V, 18 A current from the Keysight N6970A Advanced Power System to the two resistors inside the thermal chamber. Subsequently, the temperature was set by switching on and off the resistors through a relay, controlled by a PIC microcontroller illustrated in Fig. 1. (d). A thermocouple inserted onto the DUT's thermal heat tab provided temperature feedback to the microcontroller in order to actively keep the temperature constant. The DUT was kept at the desired temperature for up to 10 minutes prior any measurements were done to ensure that the DUT's junction temperature reached the temperature of the DUTs thermal heat sink. Thermally elevated tests demonstrated that the thermal chamber was accurately capable of reaching temperatures up to temperatures of 250 °C. However, the DUTs packaging limited the experiments to 175 °C.

The static characteristics for the DUT were performed using the Keysight B1505A Power Device Analyzer [14]. The thermal chamber was inserted on the 500 Amp Ultra-High Current 3-pin inline package socket module on the N1265A Ultra-High Current Expander/Fixture.

The overall representation of the experimental setup is depicted in Fig. 1. (a) In addition, it should be stated that the temperature of the thermal chamber was validated through the thermocouple from the B1505A.

B. Methodology

The DUTs were inserted into the 500 Amp Ultra-High Current 3-Pin Inline Package Socket Module and the thermal chamber was placed on top. The temperature of thermal chamber was set and allowed to stabilise to ensure an accurate uniformity within the thermal chamber. The DUTs were tested at 25 - 175 °C at 25 °C intervals to provide an appropriate range of data that is acceptable for the device limitations.

In the static characterisation of the DUTs a series of test procedures including the I-V (I_{ds}-V_{ds}), transfer characteristics (I_{ds}-V_{gs}), on-state resistance (R_{ON}) and breakdown voltage (BVDSS) measurements were setup on the B1505A and ran in the quick test environment. This therefore, required the elevation of the thermal chamber's temperatures once the set of experiments were successfully performed. In addition, the experiments applied pulsed measurements with the measurements taken at stabilised conditions to minimise the effect of self-heating on the DUT. For the Transphorm TPH3206LD 8x8 PQFN package the drain, source and gate terminals were soldered onto the package to make it compatible with the 500 Amp Ultra-High Current 3-Pin Inline Package Socket Module. All other devices did not require adjustment. For the DUTs if the parameters for the test procedure were not stated they were performed in accordance with their respective datasheets. The results of the experiments are detailed and discussed below.

Authorized licensed use limited to: Cyprus University of Technology. Downloaded on August 05,2024 at 09:50:15 UTC from IEEE Xplore. Restrictions apply.

III. Experimental Results and Discussion

The GaN-on-Si PGA26C09DV, TPH3206LD, TPH3206PD and Si SPA15N60C3 S-J power devices were characterized at elevated temperatures between 25 and 175 °C.

A. Transfer Characterisitcs

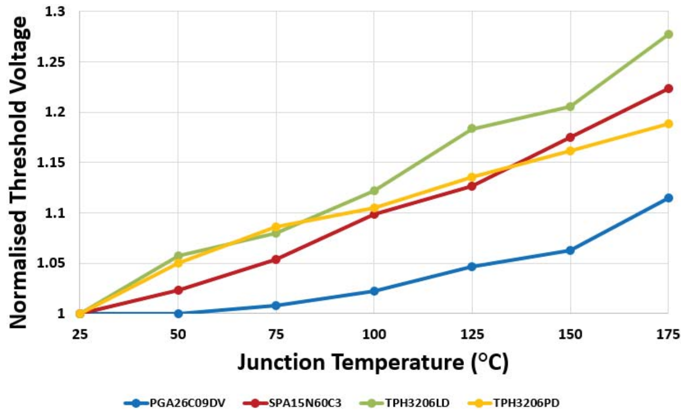

Fig. 2: Normalized threshold voltage versus junction temperature for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices.

The DUT's threshold voltage (V_{th}) was determined through linear extrapolation [15]. The thresholds were then normalized to calculate the threshold shift at elevated temperatures. In Fig. 2 the normalized threshold voltages are displayed. The Panasonic PGA26C09DV GaN-on-Si GIT demonstrates the most robust characteristics of all the DUTs with a deviation of 0.11 from 25 to 175 °C. The Transphorm TPH3206PD deviates by 0.19 and followed by the Infineon SPA15N60C3 with a deviation of 0.22 and finally the Transphorm TPH3206LD displaying a deviation of 0.28.

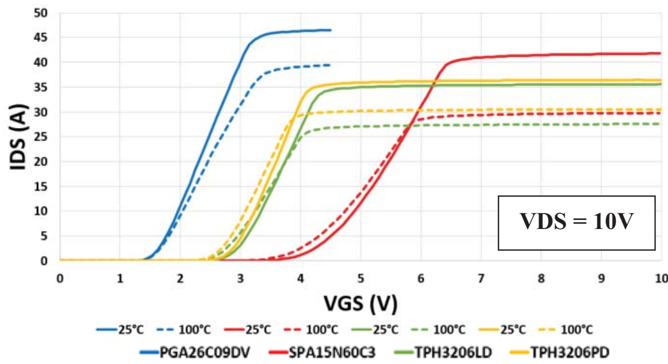

Fig. 3: Transfer Characteristics at 25 °C and 100 °C for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices.

At 25 °C the PGA26C09DV has a threshold of 1.36 V, the Transphorm TPH3206PD has a threshold voltage of 2.52 V, the TPH3206LD has a threshold voltage of 2.58 V and the Infineon SPA15N60C3 has a threshold of 3.56 V. At 100 °C the PGA26C09DV has a threshold of 1.33 V, the Transphorm TPH3206PD has a threshold voltage of 2.28 V, the TPH3206LD has a threshold voltage of 2.3 V and the Infineon SPA15N60C3 has a threshold of 3.24 V.

B. On-Resistance

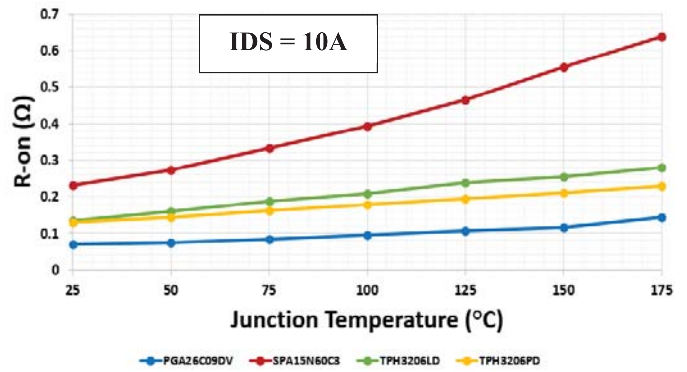

Fig. 4: On Resistance at I_{DS} = 10 A versus junction temperature for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices.

The on-state resistance was calculated for each DUT and plotted against the T_j, see Fig. 4. The PGA26C09DV GaN-on-Si GIT demonstrated the most robust and low on-state resistance. The two Transphorm GaN-on-Si HEMT devices displayed robust on-resistances with regards to their junction temperature and the Silicon SPA15N60C3 S-J displayed the highest on-state resistance and variation with temperature.

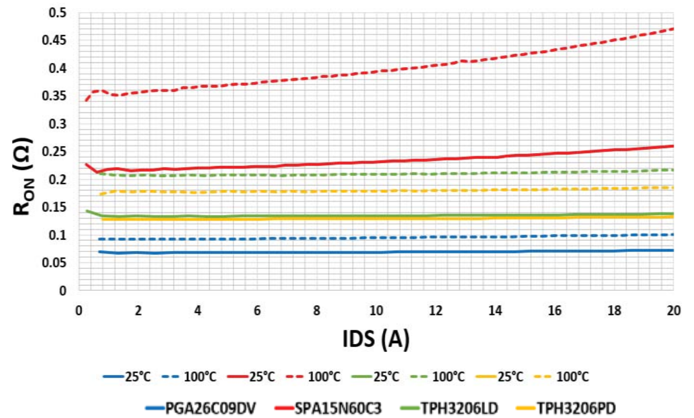

Fig. 5: On Resistance versus Drain Current at 25 °C and 100 °C for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices.

At 25 °C and a IDS of 10 A the PGA26C09DV has an on-resistance of 69 mΩ, the Transphorm TPH3206PD, 129 mΩ, the TPH3206LD, 134 mΩ and the Infineon SPA15N60C3, 232 mΩ. At 100 °C and a IDS of 10 A the PGA26C09DV has an on-resistance of 95 mΩ, the Transphorm TPH3206PD, 179 mΩ, the TPH3206LD 209 mΩ and the Infineon SPA15N60C3, 393 mΩ. The Panasonic GaN GIT operates with significantly low R_{ON} through the effect of the conductivity modulation. The p-GaN region under the gate injects holes under large gate biases and generates subsequent electrons. The mobility of electrons is far higher than that of the holes so effectively remaining stationary compared to the electrons [16].

Authorized licensed use limited to: Cyprus University of Technology. Downloaded on August 05,2024 at 09:50:15 UTC from IEEE Xplore. Restrictions apply.

C. Reverse Conduction

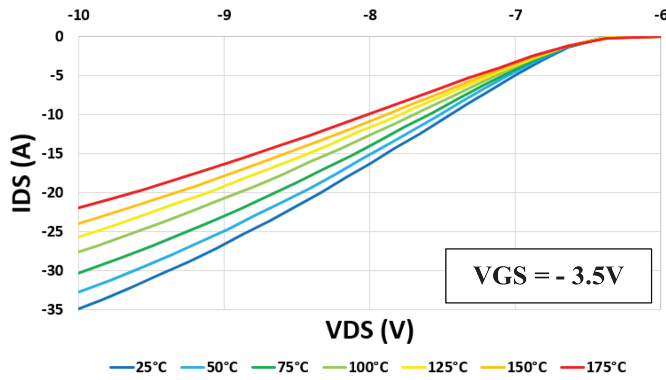

Fig. 6: Reverse conduction of the Panasonic PGA26C09DV GaN-on-Si GIT at V_{GS} = -3.5 V under different junction temperatures.

Fig. 6 displays the reverse conduction of the PGA26C09DV GIT at different junction temperatures. The E-mode GaN-on-Si devices can be employed for applications such as the half/full bridge converter [17].

D. BVDSS Measrurements

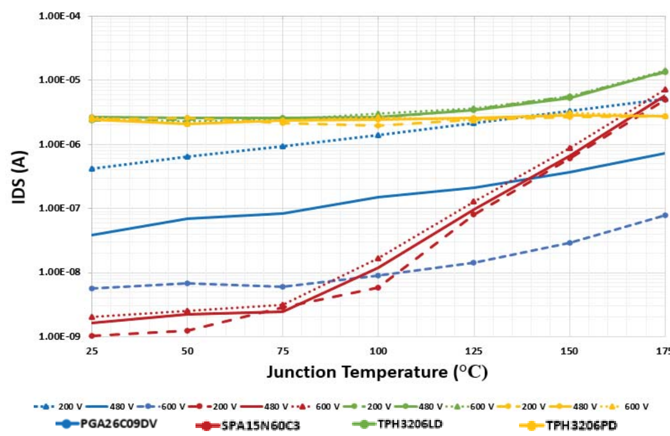

Fig. 7: Leakage current at V_{GS}= 0V under different V_{DS} biases versus junction temperature for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices.

Fig. 7 illustrates the robust nature of the leakage current in GaN-on-Si power devices in relation to temperature. Under different V_{ds} biases the leakage current for the PGA26C09DV GaN-on-Si GIT demonstrates superior leakage currents to that of traditional Silicon S-J devices. This demonstrates that under certain applications with typical T_j of 110 °C and drain biases of 200 V GaN-on-Si power devices will generate fewer power losses.

At 25 °C the PGA26C09DV has an BVDSS of 890 V, the Transphorm TPH3206PD, 1790V, the TPH3206LD, 1734 V and the Infineon SPA15N60C3, 704 V. At 100 °C the PGA26C09DV has an BVDSS of 801 V, the Transphorm TPH3206PD, 1778 V, the TPH3206LD, 1637 V and the Infineon SPA15N60C3, 747 V at 100 °C. This therefore, means that the GaN-on-Si DUTs features a negative temperature breakdown coefficient and the Si S-J features a positive temperature breakdown coefficient

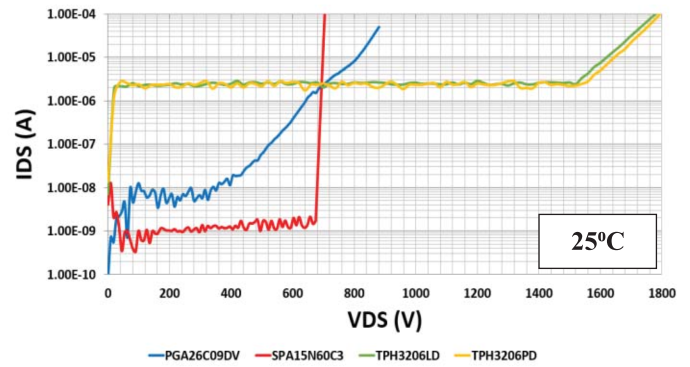

Fig. 8: BVDSS at V_{GS}= 0 V for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices at 25 °C.

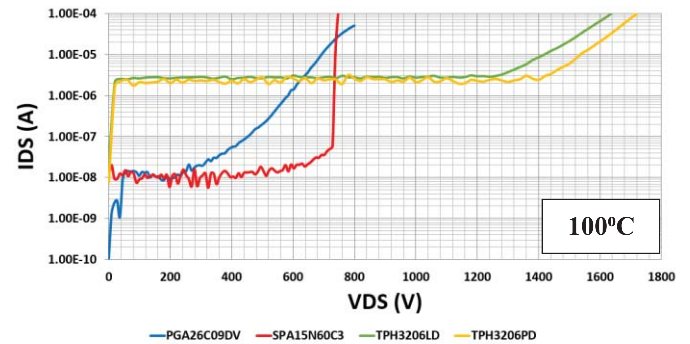

Fig. 9: BVDSS at V_{GS}= 0 V for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices at 100 °C.

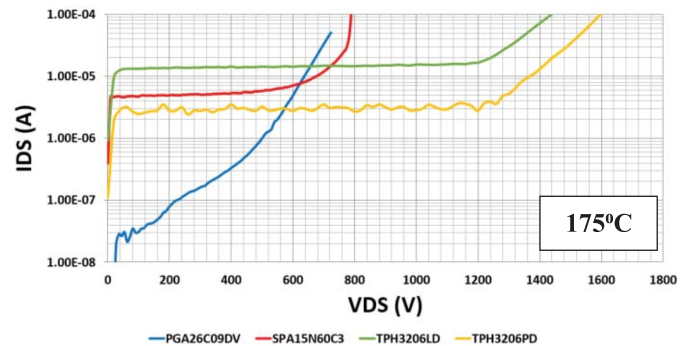

Fig. 10: BVDSS at V_{GS}= 0 V for the PGA26C09DV, SPA15N60C3, TPH3206LD and TPH3206PD devices at 175 °C.

Fig. 8, 9 and 10 display the forward blocking characteristics of the DUTs at 25 °C, 100 °C and 175 °C respectively. GaN-on-Si based power devices show extremely robust operations as temperature increases compared to that of convention Si S-J technology. GaN has a critical electric field strength of 3.3 MV as opposed to Si’s 0.2 MV [18]. This therefore, means GaN based devices do not undergo avalanche breakdown. Instead undergo Time Dependent Dielectric Breakdown (TDDB) [19].

Authorized licensed use limited to: Cyprus University of Technology. Downloaded on August 05,2024 at 09:50:15 UTC from IEEE Xplore. Restrictions apply.

IV. CONCLUSIONS

In this paper we provide the static characterization of commercial GaN-on-Si based power devices and Silicon Super Junction technology at elevated temperatures. GaN-on-Si display extreme robustness in the presence of elevated temperatures in comparison with convention Si S-J technology. The Panasonic GaN-on-Si GIT forward blocking characteristics are extremely promising in high-temperature environments even outperforming Si technology at 105 °C under a 200 V bias. Furthermore, both Transphorm GaN-on-Si devices show remarkable stability in thermally challenging environments.

Approaching 175 °C, the maximum temperature rating for the packaging the GaN-on-Si devices show excellent potential for high-temperature applications like in the oil and gas industry. The need for integration for GaN-on-Si power devices will be more apparent with the development of high-temperature capable packaging >200 °C.

In conclusion the GaN-on-Si power devices display strong stability in their performance and reliability matching if not outperforming tradition Si S-J technology.

REFERENCES

[1] A. Letellier, M. R. Dubois, J. P. Trovao, and H. Maher, "Gallium Nitride Semiconductors in Power Electronics for Electric Vehicles: Advantages and Challenges," *2015 IEEE Veh. Power Propuls. Conf.*, pp. 1–6, 2015.

[2] Y. Zhu and Y. Han, "Comparison of GaN FET and Si MOSFET based vienna rectifiers," *ECCE 2016 - IEEE Energy Convers. Congr. Expo. Proc.*, 2016.

[3] C. Liu, A. Salih, B. Padmanabhan, and W. Jeon, "Recent Progress of 650V Cascode GaN Technology," *PCIM Asia 2015; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag.*, no. May, pp. 1–8, 2015.

[4] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, 2014.

[5] S. R. Bahl, J. Joh, L. Fu, A. Sasikumar, T. Chatterjee, and S. Pendharkar, "Application reliability validation of GaN power devices," pp. 544–547, 2016.

[6] J. W. Kolar *et al.*, "PWM Converter Power Density Barriers," *2007 Power Convers. Conf. - Nagoya*, vol. L, p. P-9-P-29, 2007.

[7] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of GaN HFETs," *2nd IEEE Work. Wide Bandgap Power Devices Appl. WiPDA 2014*, pp. 24–29, 2014.

[8] S. Perkins, A. Arvanitopoulos, K. N. Gyftakis, and N. Lophitis, "A Comprehensive Comparison of the Static Performance of Commercial GaN-on-Si Devices Perkins," *IEEE 5th Work. Wide Bandgap Power Devices Appl. Albuquerque, NM.*, pp. 177–184, 2017.

[9] N. Kaminski, "The ideal chip is not enough: Issues retarding the success of wide band-gap devices," *Jpn. J. Appl. Phys.*, vol. 56, no. 4, 2017.

[10] infineon, "SPA15N60C3 Datasheet," no. Version 3.2, pp. 1–14, 2009.

[11] Panasonic, "PGA26C09DV Preliminary Datasheet," no. May, pp. 1–3, 2015.

[12] Transphorm, "TPH3206PD Datasheet," vol. 220, pp. 1–10, 2017.

[13] Transphorm, "TPH3206LD Datasheet," no. Version 2, pp. 1–8, 2015.

[14] Keysight, *Keysight B1505A Power Device Analyzer/Curve Tracer*. Keysight, 2011.

[15] F. Medjdoub, M. Van Hove, K. Cheng, D. Marcon, M. Leys, and S. Decoutere, "Novel E-Mode GaN-on-Si MOSHEMT using a selective thermal oxidation," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 948–950, 2010.

[16] Y. Uemoto *et al.*, "Gate injection transistor (GIT) - A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, 2007.

[17] G. Deboy, M. Treu, O. Haeberlen, and D. Neumayr, "Si, SiC and GaN power devices: An unbiased view on key performance indicators," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, p. 20.2.1-20.2.4, 2017.

[18] T. Paul Chow, "Wide bandgap semiconductor power devices for energy efficient systems," *WiPDA 2015 - 3rd IEEE Work. Wide Bandgap Power Devices Appl.*, pp. 402–405, 2015.

[19] T. Kachi, D. Kikuta, and T. Uesugi, "GaN Power Device and Reliability for Automotive Applications," *Int. Reliab. Phys. Symp.*, p. 3D.1.1-3D.1.4, 2012.

Authorized licensed use limited to: Cyprus University of Technology. Downloaded on August 05,2024 at 09:50:15 UTC from IEEE Xplore. Restrictions apply.