A High Frequency Phase Reference

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Abstract – Magnetic Induction Tomography (MIT) requires signal measurements with a very high degree of phase precision. To enable the development and characterisation of input amplifiers, signal distribution and signal measurement system for MIT, a high precision phase reference capable of operating over the frequency range DC - 50 MHz is being developed. The phase reference consists of two Direct Digital Synthesizers (DDS) which are supplied with a common clock and control bus. The synthesizers are programmable, allowing 14-bit resolution (20 m°) of the phase offset between the channels and 12-bit control of the output amplitude (8Vpp max). The phase reference is controlled by a PC via a USB interface. Details of the design of the phase reference and the results of measurements of the phase noise, phase drift and phase skew performance of the system is given.

Keywords – Magnetic Induction Tomography, Direct Digital Synthesis, Phase Reference

1. Introduction

Magnetic Induction Tomography (MIT) [1] is an imaging technique in which magnetic fields from an excitation coil induce eddy currents within a sample volume. These eddy currents are then sensed by receiver coils. The in-quadrature component, and hence the phase, of the received signal contains information about the conductivity of the observed sample.

The quality of the imaging will depend on the precision with which the phase can be measured. Preliminary studies suggest that a precision of 10 m° may be required for a practical biomedical MIT system at 10 MHz. [2]

The high phase precision required makes the design and development of circuitry suitable for MIT applications a difficult task. To enable the development of circuits with suitable performance for biomedical MIT, a testbench comprising a high precision phase measurement system, and a high precision, high frequency phase reference is under development by our group.

For the application of MIT system characterization and calibration, the following phase reference specifications have been set:

(i) Operational frequency range from DC to 50 MHz.
(ii) Programmable in terms of frequency, phase and amplitude.
(iii) Phase precision as close as possible to 10m°.
(iv) Amplitude can be varied completely independently of phase.
(v) Compact and lightweight design .
(vi) Control by PC via a standard bus system.

Various methods of frequency generation were considered but only Direct Digital Synthesis (DDS) could provide all the characteristics required for the phase reference.

Direct Digital Synthesis (DDS) is a digitally controlled technique for generating a tunable frequency and phase output signal from a reference frequency.

DDS offers micro Hertz tuning resolution of frequency and sub degree phase tuning capability under complete control of an external processor. Furthermore, it eliminates the need for manual system tuning and tweaking associated with component aging and temperature drift in analog synthesizer solutions.

DDS synthesizers are available in “all in one” compact packages – the devices include a sine table, DAC, and a phase-locked loop clock multiplier. This makes DDS synthesizers very easy utilize, with the minimum of external hardware required.

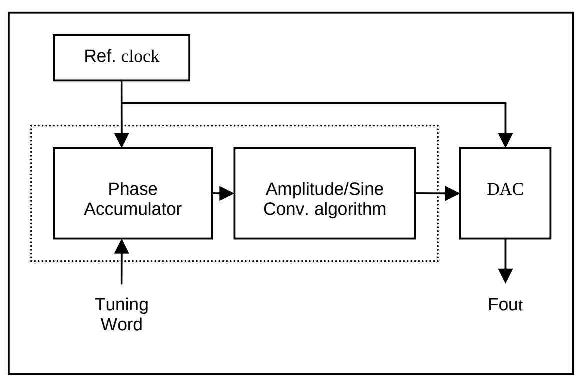

Figure1. Frequency tunable DDS system (from [3])

A phase reference system has been designed and constructed using DDS components and has undergone preliminary performance characterization measurements. This paper describes the design of the phase reference system and presents the results of the performance measurements undertaken.

2. Phase reference design

2.1 System design

The phase reference consists of three subsections:

(i) Digital synthesis section
(ii) Communication and control section
(iii) Output filtering and amplification section

Each of these subsections will be addressed separately.

2.1.1 Digital synthesis section

The core of the phase reference is the digital synthesis section which consists of two digital synthesizers' chips and supporting circuitry.

The digital synthesizer selected was the Analog Devices AD9852 which can provide an output signal frequency of up to 120MHz depending on the reference clock and the type of package used. These DDS devices are comprised of a numerically controlled oscillator, based on a sine look-up table, with a 48-bit phase accumulator. The devices also contain a reference clock multiplier which allows a low frequency external clock to produce a higher frequency internal clock. Internal 12-bit digital multipliers allow amplitude control and the sine-wave output is produced by internal 12-bit DACs. [4].

The AD9852 devices allow

- 48 bit control of frequency (~ 1µHz)
- 12 bit control of amplitude (0.5Vpp max)
- 14 bit control of phase (20m°)

The device is programmed by setting the contents of internal control registers. Control data transfer is carried out using an 8 bit parallel interface or, as has been utilized in this design, a 3-wire serial interface.

For this particular design, a 50MHz crystal oscillator module (CFPS-730, CMAC) supplied a common clock to both DDS devices, with the clock signal buffered and converted to ECL by a MC100LVEL17D differential buffer.

In order to have a well defined phase output difference, synchronization of the two digital synthesizers in terms of the output is essential.

The technique used for synchronizing the two digital synthesizers is shown in Figure3.

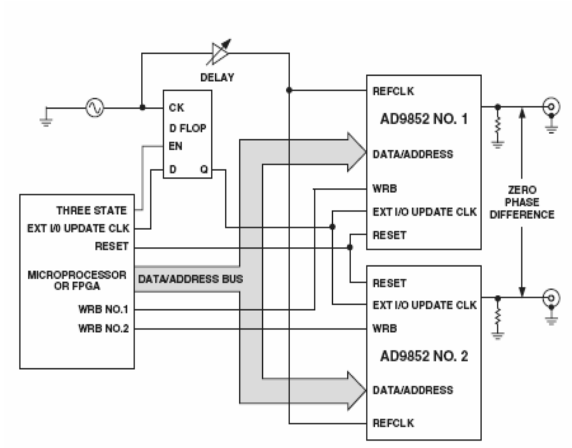

Figure 2. Synchronization of multiple AD9852 devices (from [3])

The Ext I/O command (control register update), which commands the start of operation of the AD9852, must therefore be issued to both devices simultaneously. The Ext I/O is thus synchronized with the clock using a D flip flop (74LVC1G79).

2.1.2 Communication and control section

The two synthesizers are controlled by a PIC16F877 microcontroller using serial bidirectional communication. In order to match the output of the PIC and the input of the AD9852 a 74LVT245 3.3V octal transceiver is used.

For communication between the PIC microcontroller and the PC, the Universal Serial Bus (USB) was selected because of its wide availability. A USB – serial interface (FT232, Future Devices Technology International Ltd, UK) was used for ease of implementation.

2.1.3 Output Filtering and amplification section

Due to the formation of images in the output spectrum of digital synthesizers, low pass reconstruction filters must be used. The DAC output obeys the Nyquist theorem so images are created in the output frequency spectrum at multiples of Fs ± Fo. These images compromise the quality of the output signal and must be sufficiently attenuated by reconstruction low pass filters in order to have a usable output.

The filters used in this phase reference must not only suppress the images created at the output waveform of the synthesizers but also produce minimal differential phase. The design will therefore be a compromise between the required attenuation and sufficient differential phase behavior.

Four filters were designed and tested:

(i) Active Sallen & Key 4th order Butterworth response filter
(ii) Active Sallen & Key 4th order Chebychev response filter
(iii) Passive 4th order Inverse Chebychev response filter
(iv) Passive 4th order Cauer (elliptic) response filter.

3. Measurements

3.1 Measurement objectives

The objective of these measurements was to characterize the filter stage in terms of phase noise, phase drift and phase skew and to stipulate the differential phase between the circuits under test.

Phase noise was the standard deviation of phase measured with 30 samples over 30s. Phase drift was determined to be the maximum-minimum values of phase over a period of 1 hour, taking 1800 samples. Phase skew is the variation of the output differential phase produced by varying the input signal amplitudes, while keeping the input signal differential phase offset constant. All values for phase noise, drift and skew are expressed in degrees.

3.2 Test set up

The test set up is shown in fig. 7.

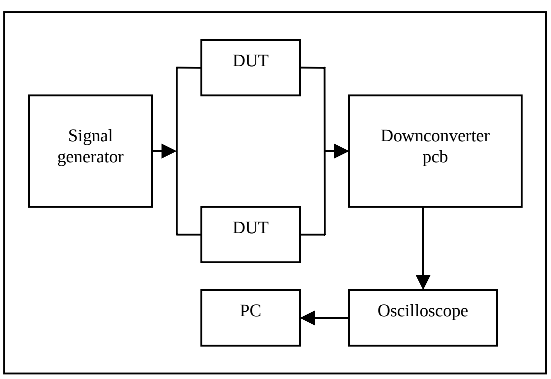

Figure 3. Test set up

The filters and the amplifier stage under test (DUT) were tested in identical pairs since in the final design each channel of the phase reference will incorporate an identical filter and amplification stage.

For the active filters, THS4275 (Texas Instruments) operational amplifiers were employed. The passive filters were constructed using surface mount inductors and capacitors (low temperature, COG).

A Marconi signal generator (model 2022C) was used to generate a sinusoidal signal to be used as input to the circuit under test. The frequency of the input signal to the circuit under test was always constant at 10.01 MHz whilst the amplitude was varied in a range from 20mV to 500mV.

The outputs of the circuit under test were passed to a 2-channel frequency down-converter stage. Here they were mixed with a 10 MHz signal derived from an crystal oscillator module to produce 10 kHz downconverted signals. The two 10 kHz signals were then fed to a comparator and the outputs of the comparators were then passed to an exclusive OR (XOR) gate. The output of the XOR was a square pulse, the width of which was assumed to be directly proportional to the differential phase between the two identical circuits under test.

The output pulse width was measured using a TDS 210 oscilloscope, and the pulse width time values were stored on a PC. The oscilloscope communicated with a PC through the GPIB interface using the Wavestar data logging program software (Tektronix).

4. Results

The results of the measurements are shown in figures 4, 5 and 6.

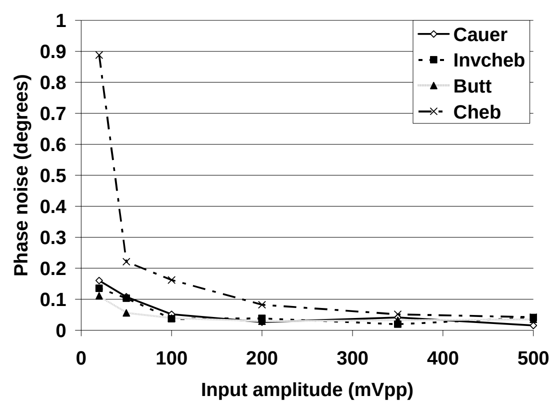

Figure 4. Phase noise graph

The phase noise was observed to decrease as the input amplitude increased. The average phase noise over the input amplitude range 20mVpp – 500mVpp for the Cauer, Inverse Chebyshev, Butterworth and Chebyshev filters was 0.067°, 0.062°, 0.050° and 0.241° respectively.

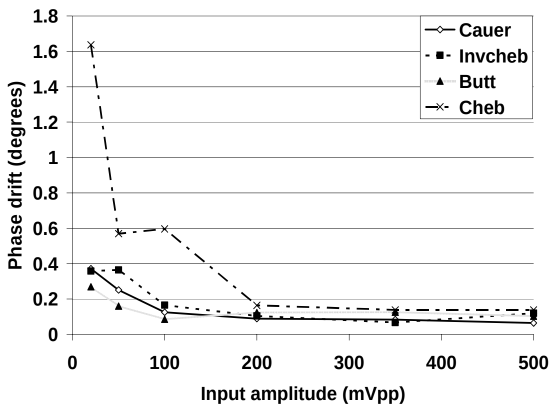

Figure 5. Phase drift graph

The phase drift was also observed to decrease as the input amplitude increased in a similar fashion to the phase noise. The average phase drift over the input amplitude range 20mVpp – 500mVpp for the Cauer, Inverse Chebyshev, Butterworth and Chebyshev filters was 0.164°, 0.196°, 0.144° and 0.540° respectively.

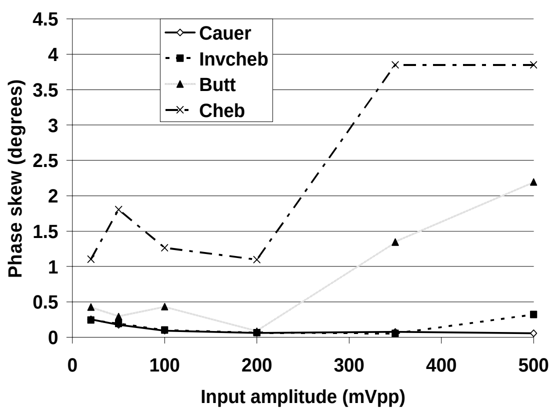

Figure 6. Phase skew graph

Phase skew was observed in all of the filter designs. The phase skew range over the input amplitude range 20mVp – 500mVpp for the Cauer, Inverse Chebyshev, Butterworth and Chebyshev filters was 0.197°, 0.267°, 2.112° and 2.753° respectively.

5. Discussion and Conclusion

The passive Cauer and Inverse Chebyshev filters and the active Butterworth produced similar performance for phase noise and phase drift. The active Chebyshev displayed inferior performance, with noise and drift of the order of 2 -3 times higher than the other types tested.

For the phase skew results, a noticeable feature was the much better performance of the passive filter designs in comparison to the active filters. Phase skew is a measure of the change in output signal phase due to changes in input amplitude. It is in principle possible to compensate for skew through programmable compensation of the output signal phase from the DDS devices. It is preferable however to minimise phase skew at source.

The passive Cauer filter appears to provide the best compromise in performance of the designs tested. One further set of measurements which is required to be carried out to fully characterise the performance of the filters, is for the image frequency attenuation to be measured, and this will now be undertaken.

Current work being undertaken includes the design and testing of the gain stage, which is required to produce 30dB of gain with phase noise, drift and skew performance similar to that observed for the Cauer filter.

The synthesiser section has undergone functionality testing and the USB and PC control software is currently being developed. Preliminary results obtained from phase precision measurements of the DDS devices, filter sections and gain stages suggest that the completed system should achieve long term phase precision of the order of <0.5° over the frequency range DC- 10MHz.

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